Bluetooth Module Datasheet

CZW-3040-02

Model:CZW-3040-02 Hardware Version: V2.0 Release Date: 2019.01.11

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1 summary

CZW-3040-02 is a Bluetooth module designed by ShenZhen Cheng Zhi Wei Technology Co.,Ltd. using Qualcomm Bluetooth chip qcc3040.

CZW-3040-02 is includes an application-dedicated Developer Processor and a system Firmware Processor that runs code from an internal flash memory. Both processors have tightly coupled memory (TCM) and an on-chip cache for performance while executing from flash memory.

CZW-3040-02 package is compatible with czw02 series pins, easy replacement and upgrade

Model Name	CZW-3040-02
Package	54 Pin Module
Dimension	13mm x 18mm x 2.4mm
Chipset	QCC3040
Bluetooth Version	Bluetooth 5.2
Power Class	Class2
Transmission Distance	≥10M
Voltage	2.8~4.2V
Temperature	-10∼+70℃
Storage Temperature	-40∼+85℃
Frequency Range	2402~2480MHz
Maximum RF Transmit Power	9dBm
π/4 DQPSK Receive Sensitivity	-91dBm
8DPSK Receive Sensitivity	-81dBm

2 General specifications

3 Key Features

3.1 Device description

- ★ Tri-core processor architecture
- ★ High-performance programmable Bluetooth[®] mono audioSoC
- ★ Low power modes to extend battery life

3.2 Features

- ★ Qualified to Bluetooth v5.1 specification
- ★ 120 MHz Qualcomm® Kalimba[™] audio DSP
- ★ 32 MHz Developer Processor for applications
- ★ Firmware Processor for system
- ★ Flexible QSPI flash programmable platform
- ★ High-performance 24- bit audio interface
- ★ Digital and analog microphone interfaces
- ★ Flexible PIO controller and LED pins with PWM support
- ★ Serial interfaces: UART, Bit Serializer (I² C/SPI), USB 2.0
- ★ Advanced audio algorithms
- ★ Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm[®]
- ★ Qualcomm[®] aptX[™] and aptX HD Audio
- ★ 1 or 2 mic Qualcomm® cVc[™] headset speech processing
- ★ Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

3.3 Audio subsystem

- ★ 32- bit Kalimba audio digital signal processor (DSP) core with flexible clocking from 2 MHz to 120 MHz to enable optimization of performance vs. power consumption
- ★ DSP executes code from ROM
- ★ 112 KB program random access memory (RAM)
- ★ 448 KB data RAM
- ★ 6 Mb ROM

3.4 Application subsystem

- ★ Dual-core application subsystem 32 MHz operation
- ★ 32- bit Firmware Processor
- ★ 32- bit Developer Processor executes:
- ★ 32 Mb flash memory
- ★ On-chip caches per core enable optimized performance and power consumption

3.5 Bluetooth subsystem

- ★ Qualified to Bluetooth v5.1 specification including 2 Mbps Bluetooth Low Energy
- ★ Single ended antenna connection with on-chip balun and Tx/Rx switch
- ★ Bluetooth, Bluetooth Low Energy, and mixed topologies supported
- ★ Class 1 support

3.6 Li-ion battery charger

- ★ Integrated battery charger supporting up to 200 mA charge current
- ★ Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V
- ★ Thermal monitoring and management are available in application software
- ★ Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V

3.7 Power management

- ★ Integrated power management unit (PMU) to minimize external components
- ★ runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)
- ★ Auto-switching between battery and USB (or other) charging source
- ★ Power islands employed to optimize power consumption for variety of use-cases
- ★ Dual switch-mode power supply

3.8 Audio engine and digital audio interfaces

- ★ 1 x unidirectional 24- bit inter-integrated circuit sound (I² S) interface
- ★ Mono analog output configurable as differential Class-AB earphone speaker output or differential high efficiency Class-D output
- ★ Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs
- ★ 1 microphone bias (single bias shared by the two channels)
- ★ Digital microphone inputs with capability to interface up to 8 digital microphones
- ★ Both analog-to-digital converter (ADC)s and the digital-toanalog converter (DAC) support sample rates of 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz. The DAC also supports 192 kHz and 384 kHz.

3.9 Peripherals and physical interfaces

- ★ A universal asynchronous receiver transmitter (UART) interface
- ★ 2 x Bit Serializers (programmable serial peripheral interface (SPI) and inter-integrated circuit interface (I² C) hardware accelerator)
- ★ 1 x USB interface
- ★ Internal NOR flash interface
- ★ Up to 22 programmable input/output (PIO) and 5 open drain/digital input light-emitting diode (LED) pads with pulse width modulation (PWM)

4 Applications

★ TrueWireless[™] stereo earbuds

5 Block Diagram



6 Module Package Information

6.1 Pinout Diagram and package dimensions



6.2 Module Pin descriptions



7 Pin Function Description

Pin#	Pin Name	Pin type	Description
1	PIO[20]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 20. Alternative function: PCM_DOUT[1]
2	PIO[19]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 19. Alternative function: PCM_DIN[0]
3	PIO[18]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 18. Alternative function: PCM_DOUT[0]
4	PIO[17]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 17. Alternative function: PCM_SYNC
5	PIO[16]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 16. Alternative function: PCM_CLK
6	PIO[15]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 15. Alternative function: MCLK_OUT
7	VBAT_SENSE	Analog	Battery voltage sense input.
8	USB_DN	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
9	USB_DP	Digital	USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection
10	VCHG	Supply	Charger input to Bypass regulator.
11	VCHG_SENSE	Analog	Charger input sense pin after external mode sense-resistor. High impedance. NOTE If using internal charger or no charger, connect VCHG_SENSE direct to VCHG.
12	NC	NC	NC
13	SYS_CTRL	Digital input	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull. Additional function: PIO[0] input only
14	VBAT	Supply	Battery voltage input.
15	GND	Ground	Ground
16	LED[0]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
17	LED[1]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.

Pin#	Pin Name	Pin type	Description
18	LED[2]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
19	LED[4]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
20	LED[5]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
21	GND	Ground	Ground
22	1V8	Supply	1.8V voltage output
23	VDD_PADS_1	Supply	1.8 V/3.3 V PIO supply.
24	VDD_PADS_3、7	Supply	1.8 V/3.3 V PIO supply.
25	PIO[4]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 4. Alternative function: TBR_MOSI[1]
26	PIO[3]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 3. Alternative function: TBR_MISO[2]
27	PIO[6]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 6. Alternative function: TBR_MOSI[0]
28	PIO[5]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 5. Alternative function: TBR_MISO[1]
29	PIO[8]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 8. Alternative function: TBR_CLK
30	PIO[7]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 7. Alternative function: TBR_MISO[0]
31	PIO[2]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 2. Alternative function: TBR_MISO[3]
32	PIO[1]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot.
33	PIO[60]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 60.
34	SPKR_N	VDD_AUDIO_HP_ SPKR	Headphone/speaker differential right output, negative. Alternative function: Differential right line output, negative
35	SPKR_P	VDD_AUDIO_HP_ SPKR	Headphone/speaker differential right output, positive. Alternative function: Differential right line output, positive
36	SPKL_N	VDD_AUDIO_HP_ SPKL	Headphone/speaker differential left output, negative. Alternative function: Differential left line output,

			negative	
Pin#	Pin Name	Pin type	Description	
37	SPKL_P	VDD_AUDIO_HP_ SPKL	Headphone/speaker differential left output, positive. Alternative function: Differential left line output,	
38	GND	Ground	Ground	
39	MIC_BIAS	VDD_AUDIO_1V8	Mic bias output.	
40	MICR_N	VDD_AUDIO_1V8	Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative	
41	MICR_P	VDD_AUDIO_1V8	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive	
42	MICL_N	VDD_AUDIO_1V8	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative	
43	MICL_P	VDD_AUDIO_1V8	Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive	
44	GND	Ground	Ground	
45	GND	Ground	Ground	
46	BT_RF	VDD_BT_RADIO	Bluetooth transmit/receive.	
47	GND	Ground	Ground	
48	PIO[14]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 14	
49	PIO[13]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 13	
50	PIO[12]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 12	
51	PIO[11]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 11	
52	PIO[10]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 10	
53	PIO[9]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 9	
54	PIO[21]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 21. Alternative function: PCM_DOUT[2]	

8 Reference application circuit



Notice: for reference only, please design the circuit according to the actual application

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Rating	Minimum	Maximum
Storage temperature	-40 ℃	+85℃

9.2 Recommended Operating Conditions

Operating Condition	Minimum	Maximum
Operating temperature range	-40 ℃	+85℃
Supply voltage: VBAT	+2.8V	+4.3V

10 Recommended reflow temperature profile



The module Must go through 100 $^\circ\!\!\!\!{}^\circ\!\!\!{}^\circ$ baking for at least 12 hours before SMT AND IR reflow process!

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