Features

- Single-chip mono headset solution with advanced echo and noise cancellation
- Packet/bit error correction to improve audio quality due to air interference
- Programmable audio prompts
- Low power consumption: over 13 hours talk time from a 120mAh battery
- High-performance CVC single-microphone echo and noise cancellation
- Advanced Multipoint support: allows a headset (HFP) connection to 2 phones for voice
- Secure Simple Pairing and Proximity Pairing (headset initiated pairing)
- Best-in-class Bluetooth radio with 8.5dBm transmit power and -91dBm receive sensitivity
- 64MIPS Kalimba DSP coprocessor
- Configurable mono headset software
- HFP v1.5 and HSP v1.1 support
- 1.5V and 1.9V linear regulators
- Switch-mode regulator
- 150mA lithium battery charger
- High-quality mono codec with 95dB SNR DAC
- 48-lead 7 x 7 x 0.9mm, 0.5mm pitch QFN, pin compatible with BlueVox2 QFN and BC6130 QFN
- Green (RoHS compliant and no antimony or halogenated flame retardants)

BC6140 QFN

BC6140 QFN Low-cost Mono DSP Headset Solution

Fully Qualified Single-chip Bluetooth® v2.1 + EDR System

Production Information

BC6140A02

Issue 4

General Description

BC6140 QFN is a product from CSR's Connectivity Centre. It is a low-cost fully featured ROM IC solution for mono headsets with extremely low power consumption. BC6140 QFN is the first CSR solution to include improved packet/bit error correction, a CSR solution to reduce noise and interference at the near-end enabling the headset-user to enjoy superior audio quality.

BC6140 QFN reduces the number of external components required ensuring production costs are minimised. It includes a Bluetooth radio, baseband, Kalimba DSP, DAC/ADC, switch-mode power supply and battery charger in a compact QFN package for low-cost designs.

BC6140 QFN contains the Kalimba DSP coprocessor for supporting enhanced audio applications.

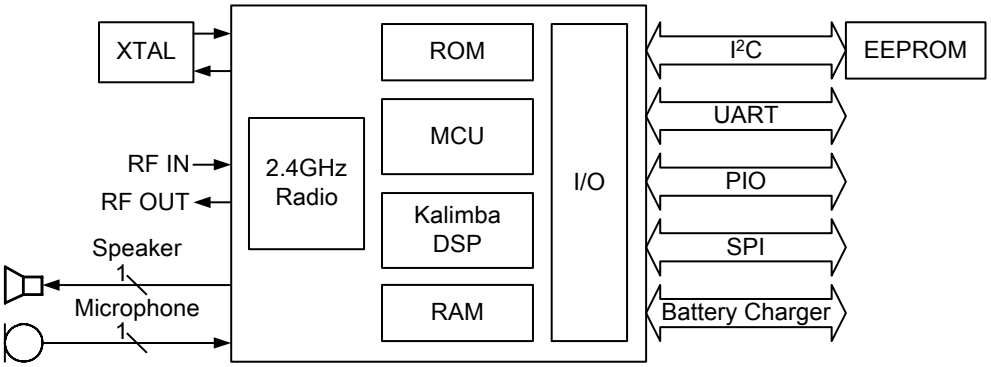
Applications

- Low-cost mono DSP headset

BC6140 QFN includes state-of-the-art CVC single-microphone echo and noise reduction, which reduces headset echo allowing the headset-user to be heard more clearly. Advanced Multipoint enables HFP connection to 2 phones simultaneously, enhancing the use case for voice.

BC6140 QFN supports Secure Simple Pairing which simplifies the pairing process and makes it easier to use a Bluetooth headset.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.



Document History

Revision	Date	Change Reason
1	26 JAN 09	Original publication of this document
2	10 JUN 09	New package added and part changed to A02. Proximity Pairing added. Various minor editorial updates.
3	12 JUN 09	Feature-set confirmed.
4	31 JUL 09	Production Information, includes ESD, Power Consumption figures and talk time value added. Irrelevant SBC figure removed. EEPROM size note for programmable audio prompts added. Minor editorial changes. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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BC6140 QFN devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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Refer to www.csrsupport.com for compliance and conformance to standards information.

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1 Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant

Transmitter

- 8.5dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range typically >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -91dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 26MHz

Baseband and Software

- Internal ROM
- 48KB of internal RAM, allows full-speed data transfer, mixed voice/data and full Piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air
- Configurable mono headset ROM software to set-up headset features and user interface
- Support for HFP v1.5 (including three-way calling) and HSP v1.1
- Support for Bluetooth v2.1 + EDR specification Secure Simple Pairing
- Proximity Pairing (headset initiated pairing)
- Packet Loss Concealment and Bit Error Concealment to improve audio quality in the presence of air interference
- Advanced Multipoint support, allowing the headset to connect to 2 mobile phones or 1 mobile phone and a VoIP dongle
- DSP based single-microphone CVC echo and noise cancellation is included in the BC6140 QFN for effective noise cancellation under all conditions
- BC6140 QFN low-cost mono DSP headset solution development kit available, includes example design. Order code DK-BC-6140-1A

Kalimba DSP

- Very low power Kalimba DSP coprocessor, 64MIPS, 24-bit fixed point core
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 4K x 32-bit program RAM, 8K x 24-bit + 4K x 24-bit data RAM
- 64 x 32-bit program memory cache when executing from ROM

Audio Codec

- 16-bit resolution mono codec
- Integrated amplifiers for driving a 16Ω speaker; no need for external components
- Support for single-ended speaker termination and line output
- Integrated low-noise microphone bias
- Digital enhancements to add bass cut and side tone
- Analogue enhancements to support single-ended speaker drive capability and reference availability

Physical Interfaces

- Synchronous serial interface for system debugging
- I²C compatible interface used to communicate with an external EEPROM which contains all of the device configuration (PS Keys)
- UART interface with data rates up to 3Mbits/s

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Device can run in low power modes from an external 32.768kHz clock signal
- Programmable audio prompts
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- On-chip regulators: 1.5V output from 1.7V to 2.8V input and 1.9V output from 2.7V to 5.5V input
- On-chip high-efficiency switch-mode regulator; 1.5V output from 2.2V to 4.4V input
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies permitted
- 10-bit ADC
- Battery charger with programmable current, 20mA to 150mA for lithium ion/polymer battery
- 2 LED drivers with faders

Package Option

- 48-lead 7 x 7 x 0.9mm, 0.5mm pitch QFN

2 Functional Block Diagram

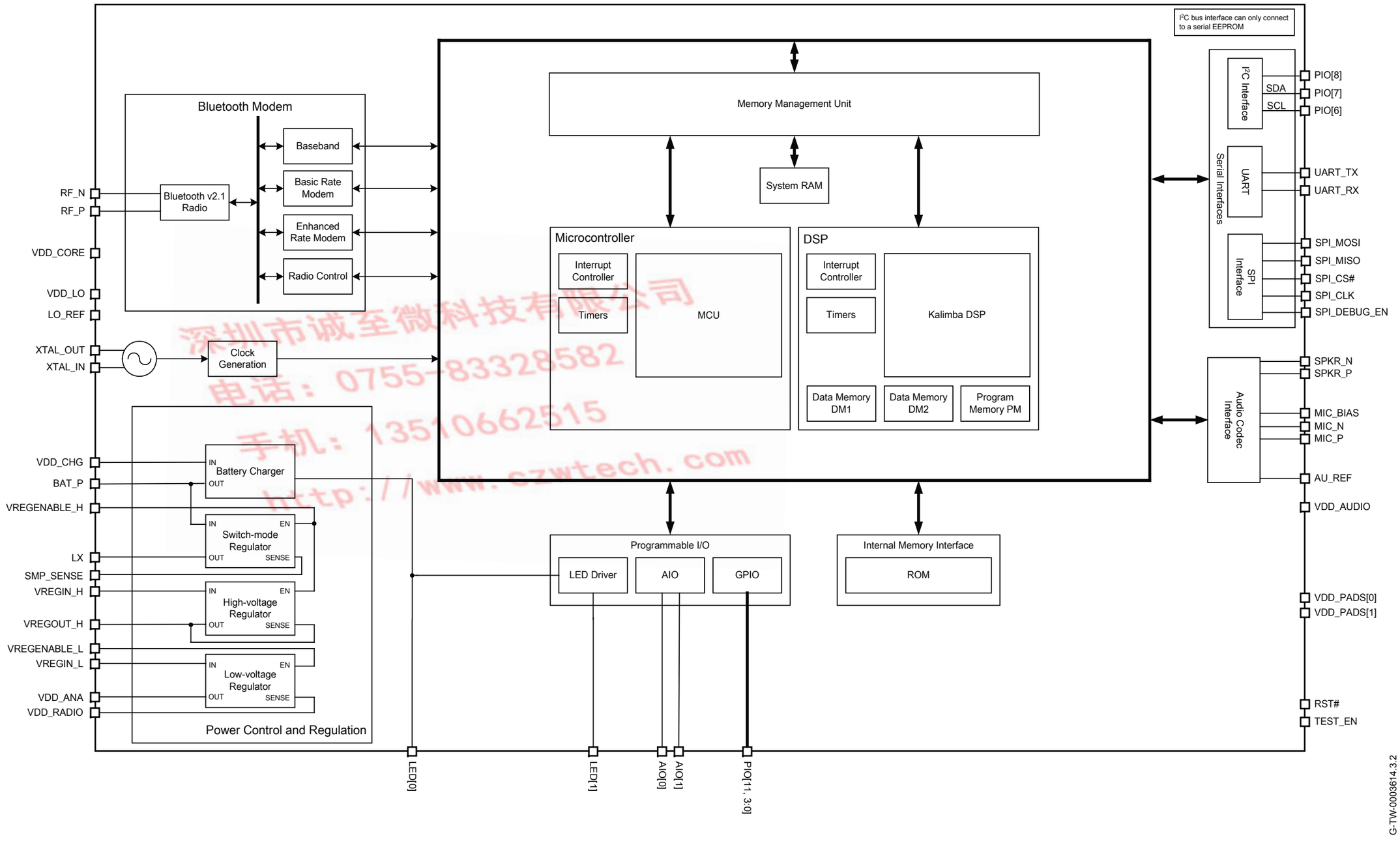

Figure 2.1: Functional Block Diagram

3 Package Information

3.1 Pinout Diagram

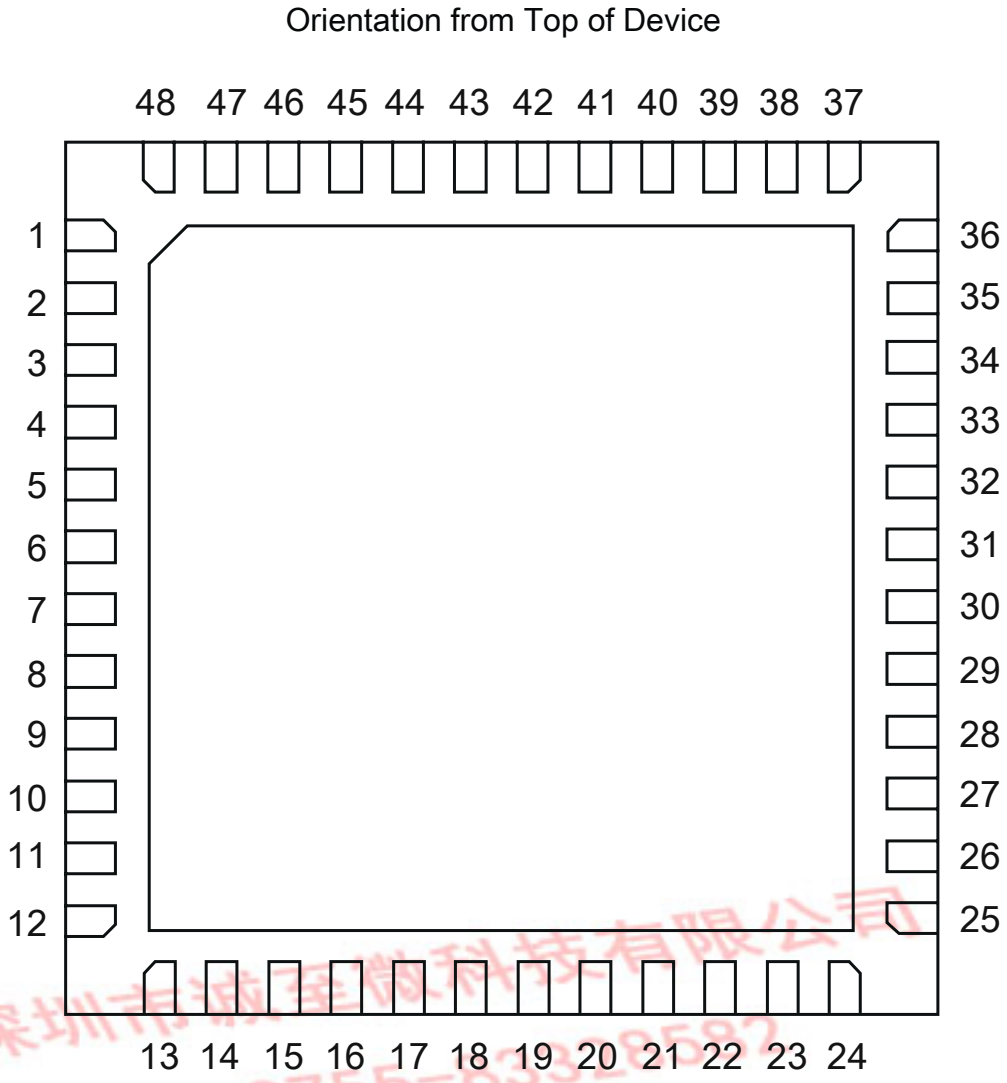

Figure 3.1: Device Pinout

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3.2 Device Terminal Functions

Bluetooth Radio	Lead	Pad Type	Supply Domain	Description
RF_N	8	RF	VDD_RADIO	Transmitter output/switched receiver
RF_P	7	RF	VDD_RADIO	Complement of RF_N

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	13	Analogue	VDD_ANA	For crystal or external clock input
XTAL_OUT	14	Analogue	VDD_ANA	Drive for crystal
LO_REF	15	Analogue	VDD_ANA	Reference voltage to decouple the synthesiser

SPI Interface	Lead	Pad Type	Supply Domain	Description
SPI_MOSI	38	Input, with weak internal pull-down	VDD_PADS[1]	SPI data input
SPI_CS#	40	Bidirectional with weak internal pull-down	VDD_PADS[1]	Chip select for SPI, active low
SPI_CLK	39	Bidirectional with weak internal pull-down	VDD_PADS[1]	SPI clock
SPI_MISO	41	Bidirectional with weak internal pull-down	VDD_PADS[1]	SPI data output
SPI_DEBUG_EN	42	Input with strong internal pull-down	VDD_PADS[1]	Enable for debug interface, active high. Must be enabled before SPI_CS#.

UART Interface	Lead	Pad Type	Supply Domain	Description
UART_TX	19	Bidirectional with weak internal pull-up	VDD_PADS[0]	UART data output, active high
UART_RX	18	Bidirectional with weak internal pull-down	VDD_PADS[0]	UART data input, active high

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[11]	27	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[0]	Programmable input/output line
PIO[8]	44	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[1]	Programmable input/output line
PIO[7]	45			
PIO[6]	46			
PIO[3]	21	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[0]	Programmable input/output line
PIO[2]	22			
PIO[1]	23			
PIO[0]	24			
AIO[0]	17	Bidirectional	VDD_ANA	Programmable input/output line
AIO[1]	16			

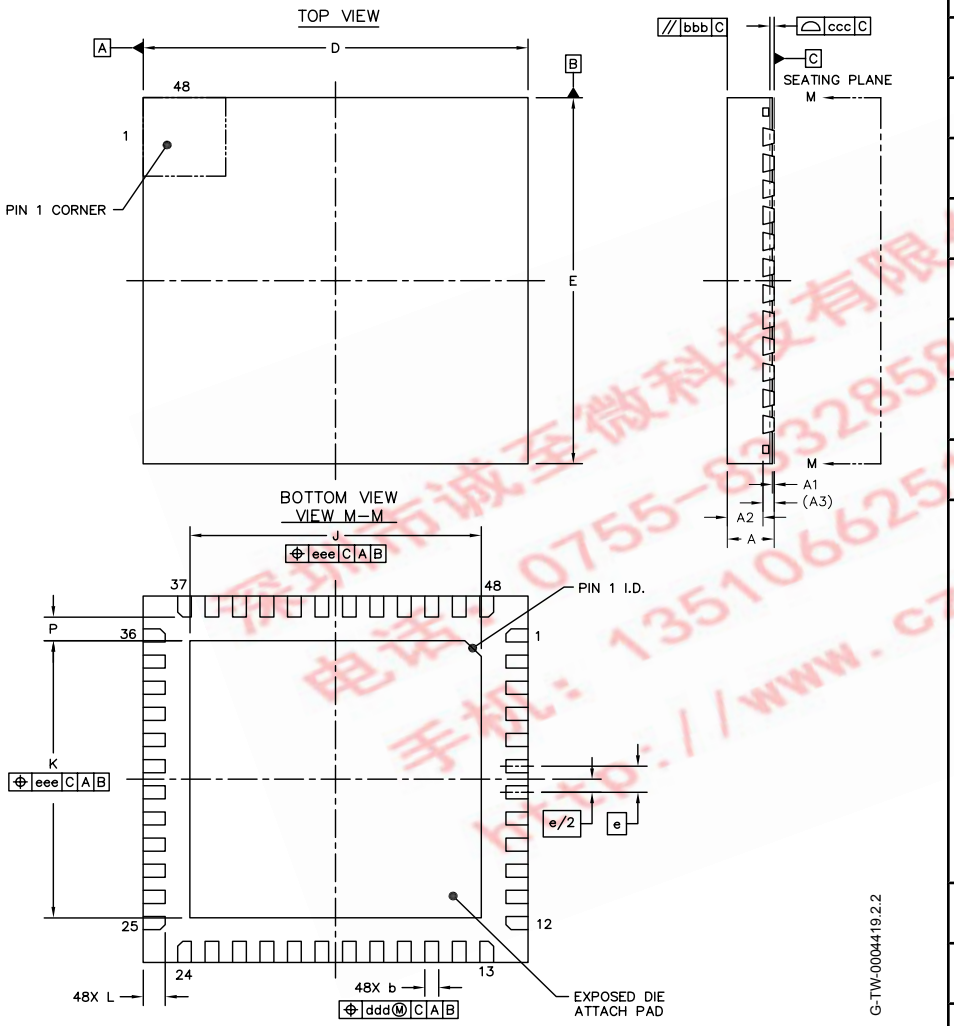
Audio	Lead	Pad Type	Supply Domain	Description
SPKR_N	3	Analogue	VDD_AUDIO	Speaker output, negative
SPKR_P	4	Analogue	VDD_AUDIO	Speaker output, positive
MIC_N	2	Analogue	VDD_AUDIO	Microphone input, negative
MIC_P	1	Analogue	VDD_AUDIO	Microphone input, positive
MIC_BIAS	47	Analogue	VDD_AUDIO, BAT_P	Microphone bias
AU_REF	5	Analogue	VDD_AUDIO	Decoupling of audio reference (for high quality audio)

LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[1]	28	Open drain output	Open drain	LED driver
LED[0]	29	Open drain output	Open drain	LED driver

Test and Debug	Lead	Pad Type	Supply Domain	Description
RST#	26	Input with weak internal pull-up	VDD_PADS[0]	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	25	Input with strong internal pull-down	VDD_PADS[0]	For test purposes only (leave unconnected)

Power Supplies Control	Lead	Description
VREGENABLE_L	10	Take high to enable low-voltage regulator
VREGENABLE_H	33	Take high to enable both high-voltage regulator and switch-mode regulator
VREGIN_L	11	Input to internal low-voltage regulator
VREGIN_H	32	Input to internal high-voltage regulator
LX	35	Switch-mode power regulator output
VREGOUT_H	31	High-voltage regulator output
VDD_PADS[1]	43	Positive supply for digital input/output ports including PIO[8:6] and SPI interface
VDD_PADS[0]	20	Positive supply for digital input/output ports including PIO[11,3:0]
VDD_CORE	30	Positive supply for internal digital circuitry
VDD_RADIO	6	Positive supply for RF circuitry
VDD_ANA	12	Positive supply for analogue circuitry, AIO[1:0]. Output from internal 1.5V regulator
VDD_LO	9	Positive supply for local oscillator circuitry
VDD_AUDIO	48	Positive supply for audio
BAT_P	36	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator
VDD_CHG	37	Lithium ion/polymer battery charger input
SMP_SENSE	34	Positive supply for switch-mode control circuitry
VSS	Exposed Pad	Ground connections

3.3 Package Dimensions



Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.8	0.85	0.9	J	5.2	5.3	5.4
A1	0	0.035	0.05	K	5.2	5.3	5.4
A2	-	0.65	0.67	L	0.35	0.4	0.45
A3	-	0.203	-	bbb	-	0.1	-
b	0.2	0.25	0.3	ccc	-	0.08	-
D	6.9	7	7.05	ddd	-	0.1	-
E	6.9	7	7.05	eee	-	0.1	-
e	-	0.5	-	P	0.3	-	-

Notes

1. Coplanarity applies to leads, corner leads and die attach pad.
2. Exposed die attach pad smaller than BlueVox2 QFN. Dimensions have been reduced to enhance solderability. Backward pin-for-pin compatibility with BlueVox2 QFN is maintained

Description	48-lead Quad Flat No-lead Package		
Size	7 x 7 x 0.9mm	**JEDEC**	MO-220
Pitch	0.5	**Units**	mm

3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 7 x 7 x 0.9mm QFN 48-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern to be in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

3.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth Modem

4.1 RF Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

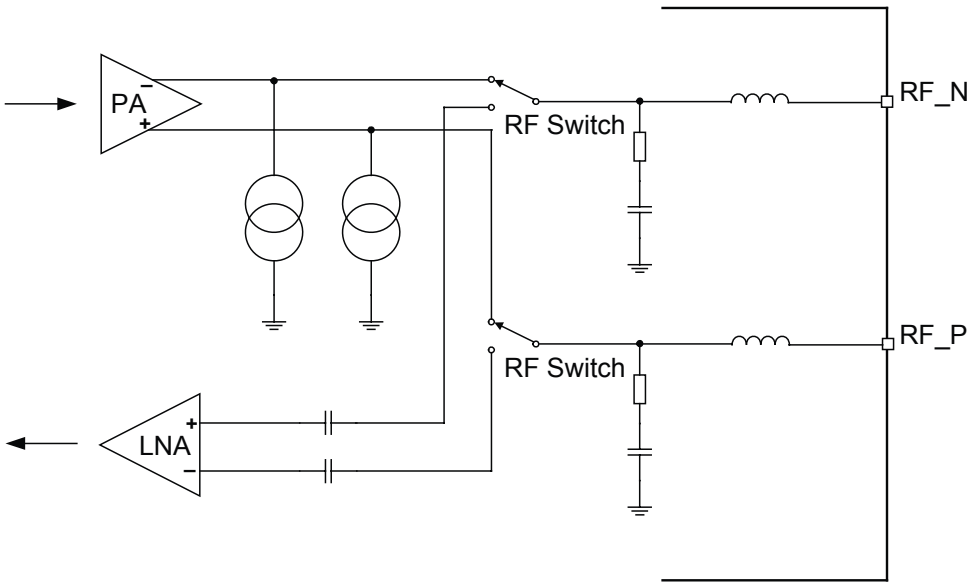


Figure 4.1: Simplified Circuit RF_N and RF_P

RF_N and RF_P require an external DC bias. The DC level must be set at VDD_RADIO.

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die.

The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BC6140 QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BC6140 QFN to be used in Class 2 and Class 3 radios without an external RF PA.

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

Including the basic rate modem allows BC6140 QFN compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BC6140 QFN supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR uses the same 1.6kHz slot rate and the 1MHz symbol rate defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3 bits. This is achieved using 2 new distinct modulation schemes. Table 4.1 and Figure 4.2 summarise these. Link Establishment and Management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF ports, receiver, transmitter and synthesiser, with the baseband components described in Section 4.5.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.1: Data Rate Schemes

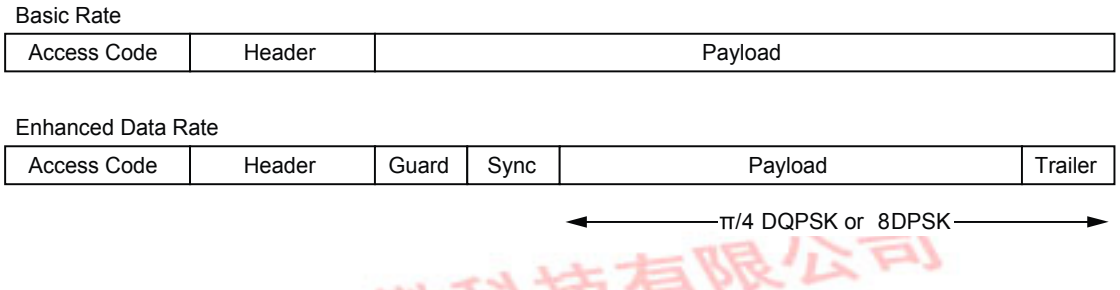


Figure 4.2: BDR and EDR Packet Structure

5 Clock Generation

BC6140 QFN requires a Bluetooth reference clock frequency, it derives this from an externally connected crystal in the range 16MHz to 26MHz.

All BC6140 QFN internal digital clocks are generated using a phase locked loop, locked to the frequency of the external reference clock.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

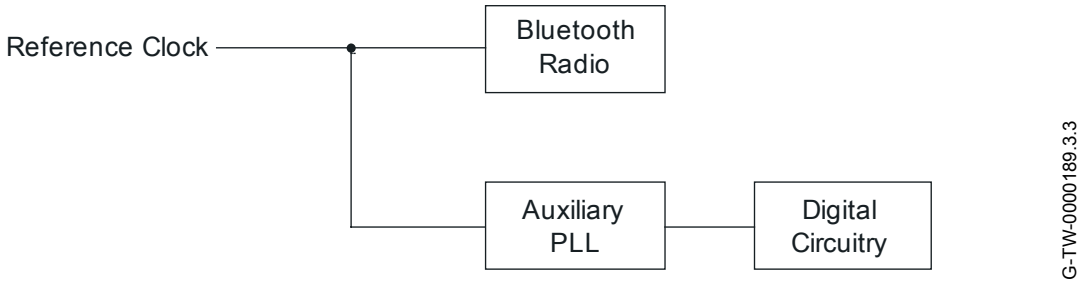


Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BC6140 QFN is configured to operate with a chosen reference frequency. This reference frequency is set by PSKEY_ANA_FREQ for all frequencies using an integer multiple of 250kHz. The input frequency default setting for BC6140 QFN is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

5.3 Crystal Oscillator: XTAL_IN and XTAL_OUT

BC6140 QFN contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 5.2 shows the external crystal is connected to pins XTAL_IN, XTAL_OUT.

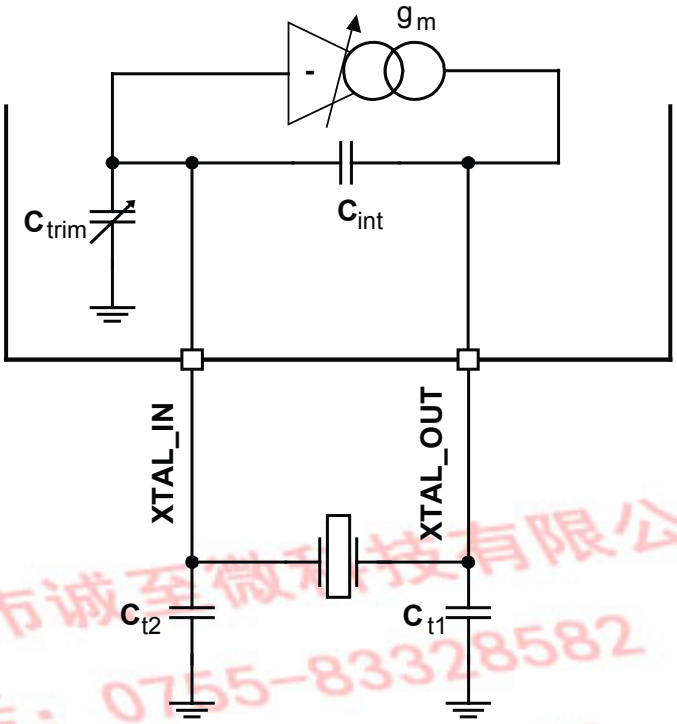


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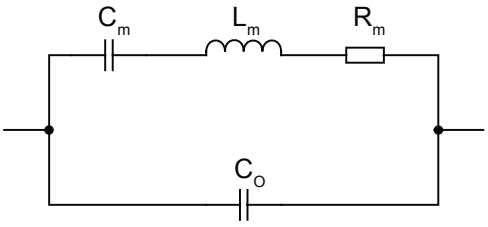
Figure 5.2: Crystal Driver Circuit

Figure 5.3 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.



G-TW-0000245.4.4

Figure 5.3: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BC6140 QFN contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	26	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 5.1: Crystal Specification

The BC6140 QFN driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.3.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BC6140 QFN provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated using Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.3.2 Frequency Trim

BC6140 QFN enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 5.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = pullability \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(ppm/LSB)$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \cdot \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 5.3

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.3.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BC6140 QFN uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\ \frac{(2\pi F_x)^2\ R_m\ ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\ (C_{t2} + C_{trim}))}{C_{t1}\ (C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BC6140 QFN guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.3.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BC6140 QFN crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it using Equation 5.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 5.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BC6140 QFN driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.3.5 Crystal PS Key Settings

The BC6140 QFN firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

BC6140 QFN should be configured to operate with the chosen reference frequency.

5.4 External 32kHz Clock

A 32kHz clock can be applied to AIO[0] by setting DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.

If the external clock is applied to the analogue pad AIO[0], the digital signal should be driven with a maximum 1.5V.

Note:

If the 32kHz clock is accurate and stable to within 200ppm, then further power saving features can be enabled. See the relevant software release note for more information.

6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 Programmable I/O (PIO) Parallel Ports

8 lines of programmable bidirectional I/O are provided.

Note:

PIO[11,3:0] are powered from VDD_PADS[0] and PIO[8:6] are powered from VDD_PADS[1]. AIO[1:0] are powered from VDD_ANA.

Any of the PIO lines are configurable as button inputs or control outputs. Certain PIOs also have dedicated functions that are accessed using appropriate PS Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful in detecting when BC6140 QFN is entering or leaving deep sleep.

Note:

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BC6140 QFN has 2 general-purpose analogue interface pins, AIO[1:0], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (output from AIO[0] only) and the XTAL and XTAL/2 clock frequency (output from AIO[1] and AIO[0]). When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

7 Kalimba DSP

The Kalimba DSP is an open platform Kalimba DSP allowing signal processing functions to be performed on over-air data or codec data in order to enhance audio applications. Figure 7.1 shows the Kalimba DSP interfaces to other functional blocks within BC6140 QFN.

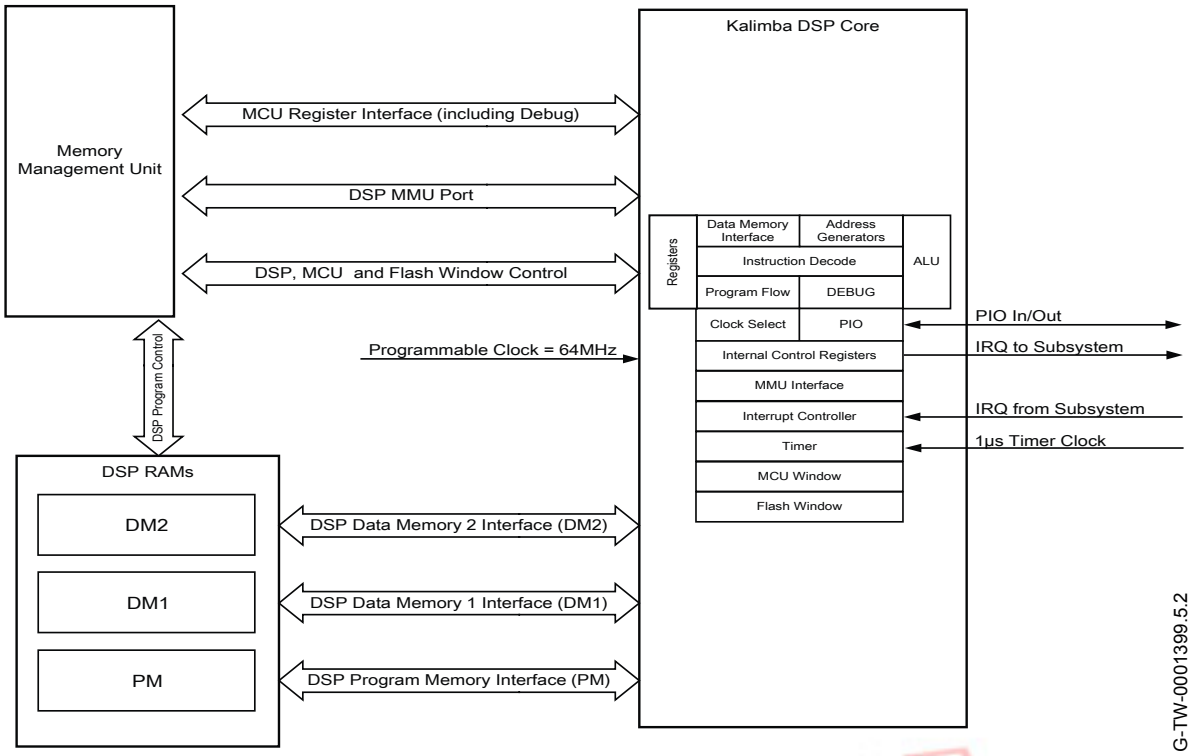


Figure 7.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 64MIPS performance, 24-bit fixed point DSP core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

8 Memory Interface and Management

8.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

8.3 Kalimba DSP RAM

Additional on-chip RAM is provided to support the Kalimba DSP:

- 8K x 24-bit for data memory 1 (DM1)
- 4K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

Note:

The Kalimba DSP can also execute directly from internal ROM, using a 64-instruction on-chip cache.

8.4 Internal ROM

Internal ROM is provided for system firmware implementation.

9 Serial Interfaces

9.1 UART Interface

BC6140 QFN has a standard UART serial interface that provides a simple communications channel for test and debug using RS232 protocol.

2 signals implement the UART function, UART_TX and UART_RX. When BC6140 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

UART configuration parameters, such as baud rate and packet format, are set using BC6140 QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 9.1: Possible UART Settings

The UART interface can reset BC6140 QFN on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 9.1. If t_{BRK} is longer than the value, defined by the HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature allows a host to initialise the system to a known state. Also, BC6140 QFN can emit a break character that may be used to wake the host.

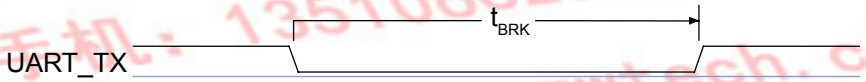


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Figure 9.1: Break Signal

Table 9.2 shows a list of commonly used baud rates and their associated values for the UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range can be set in UART_BAUDRATE according to the formula in Equation 9.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 9.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 9.2: Standard Baud Rates

9.1.1 UART Configuration While Reset is Active

The UART interface for BC6140 QFN is tristate while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BC6140 QFN reset is de-asserted and the firmware begins to run.

9.2 Programming and Debug Interface

Important Note:

SPI_DEBUG_EN must be pulled high before the SPI debug port is enabled.

The SPI is used to configure (using PS Keys) and debug the BC6140 QFN. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

BC6140 QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions can occur when the internal processor is running or is stopped. For more information, see the *Using SPI Design Guide*.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

9.2.1 Instruction Cycle

The BC6140 QFN is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 9.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 9.3: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BC6140 QFN on the rising edge of the clock line SPI_CLK. When reading, BC6140 QFN replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BC6140 QFN offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.2.2 Multi-slave Operation

BC6140 QFN should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BC6140 QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BC6140 QFN outputs `0` if the processor is running or `1` if it is stopped.

9.3 I²C Interface

PIO[8:6] is available to form a master I²C interface. The interface is formed using software to drive these lines.

Note:

The program memory for the BC6140 QFN is internal ROM so the I²C interface can only connect to a serial EEPROM, an example is shown in Figure 9.2. The EEPROM stores programmable audio prompts, see Section 16.4, as well as PS Keys and configuration information. The programmable audio prompts option requires a larger EEPROM than used in Figure 9.2, up to 512Kb.

EEPROM Supply in Figure 9.2 is 1.9V.

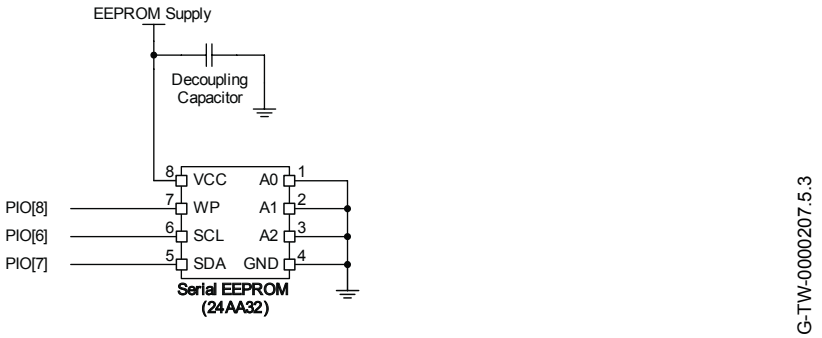

Figure 9.2: Example EEPROM Connection

10 Audio Interface

The audio interface circuit consists of:

- Mono audio codec
- Audio inputs and outputs

10.1 Audio Input and Output

The audio input circuitry consists:

- 1 channel of microphone input
- The microphone input is configurable to be either single-ended or fully differential
- The input has an analogue and digital programmable gain stage for optimisation of different microphones

The audio output circuitry consists of a single differential class A-B output stage.

10.2 Mono Audio Codec Block Diagram

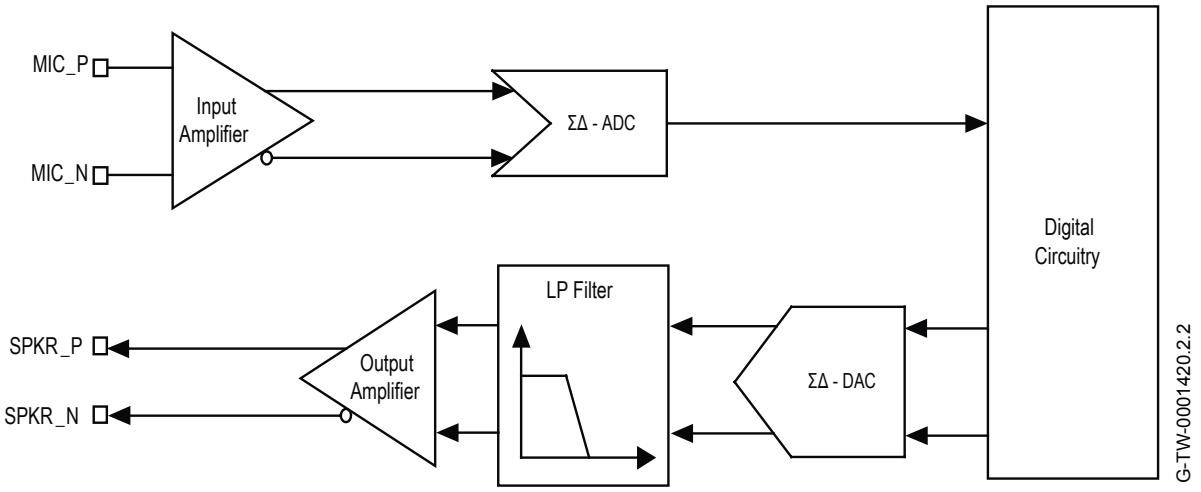

Figure 10.1: Mono Codec Audio Input and Output Stages

The mono audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

10.3 ADC

The ADC consists of:

- A second-order Sigma-Delta converter, as Figure 10.1 shows.
- 2 gain stages; one of which is an analogue gain stage and the other is a digital gain stage.

10.3.1 ADC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 10.1. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.1: ADC Digital Gain Rate Selection

10.3.2 ADC Analogue Gain

Figure 10.2 shows the equivalent block diagram for the ADC analogue amplifier. It is a two-stage amplifier:

- The first stage amplifier has a selectable gain of either bypass for line input mode or gain of 24dB gain for the microphone mode.
- The second stage has a programmable gain with 7 individual 3dB steps. By combining the 24dB gain selection of the microphone input with the 7 individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The the BC6140 QFN controls all the gain control of the ADC.

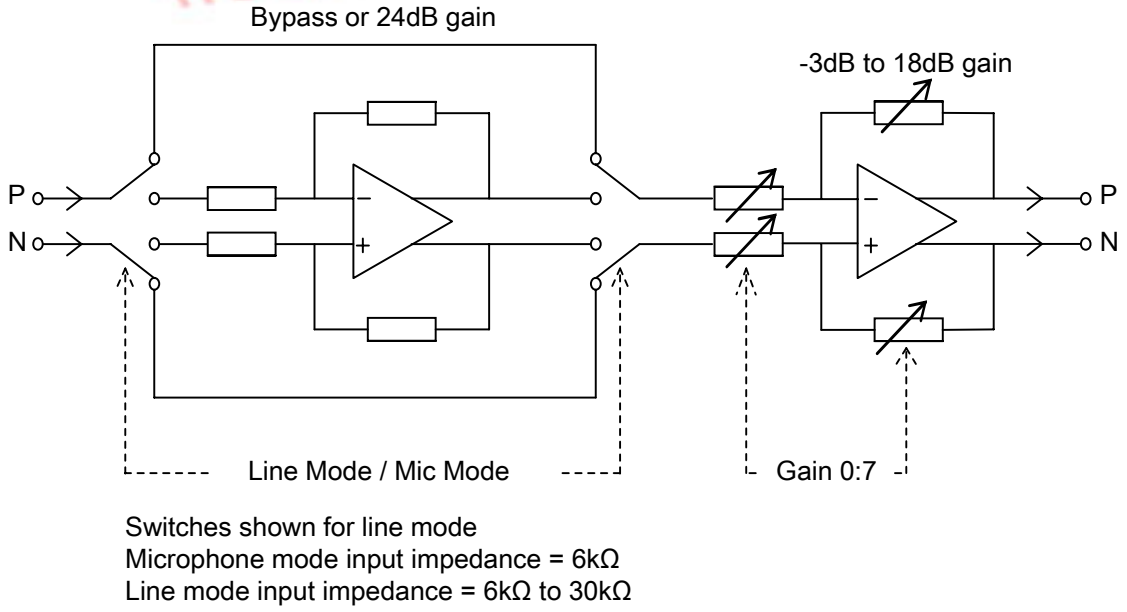

Figure 10.2: ADC Analogue Amplifier Block Diagram

10.4 DAC

The DAC consists of:

- A second-order Sigma-Delta converter, as Figure 10.1 shows.
- 2 gain stages; one of which is an analogue gain stage and the other is a digital gain stage.

10.4.1 DAC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings, summarised in Table 10.2. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

The overall gain control of the DAC is controlled by the BC6140 QFN. Its setting is a combined function of the digital and analogue amplifier settings.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.2: DAC Digital Gain Rate Selection

10.4.2 DAC Analogue Gain

As Table 10.3 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The the BC6140 QFN controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	3	3	-9
6	0	2	-12
5	-3	1	-15
4	-6	0	-18

Table 10.3: DAC Analogue Gain Rate Selection

10.5 Microphone Input

Figure 10.3 shows recommended biasing for each microphone. The microphone bias, MIC_BIAS, derives its power from the BAT_P and requires a 1µF capacitor on its output.

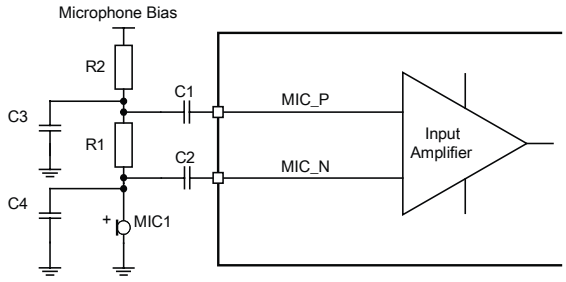

Figure 10.3: Microphone Biasing

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS maintains regulation within the limits 0.200mA to 1.230mA. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

The audio input is intended for use in the range from 1µA @ 94dB SPL to about 10µA @ 94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV.

The input impedance at MIC_N and MIC_P is typically 6.0kΩ.

C1 and C2 should be 150nF if bass roll-off is required to limit wind noise on the microphone.

R1 sets the microphone load impedance and is normally in the range of 1kΩ to 2kΩ.

R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the MIC_BIAS output (which is ground referenced and provides good rejection of the supply), which may be configured to provide bias only when the microphone is required.

Table 10.4 shows the 4-bit programmable output voltage that the microphone bias provides, and Table 10.5 shows the 4-bit programmable output current.

The characteristics of the microphone bias include:

- Power supply:
  - BC6140 QFN microphone supply is BAT_P
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.4V
  - Typically the microphone bias is between 2V and 2.5V, or as specified by the microphone vendor
- Drop-out voltage:
  - 300mV minimum
  - Guaranteed for configuration of voltage or current output shown in Table 10.4 and Table 10.5
- Output voltage:
  - 4-bit programmable between 1.7V to 3.6V
  - Tolerance 90 to 110%
- Output current:
  - 4-bit programmable from 200µA to 1.230mA
  - Maximum current guaranteed to be >1mA
- Load capacitance:
  - Unconditionally stable for 1µF ± 20% and 2.2µF ± 20% pure C

Output Step	VOL_SET[3:0]	Min	Typ	Max	Units
0	0000	-	1.71	-	V
1	0001	-	1.76	-	V
2	0010	-	1.82	-	V
3	0011	-	1.87	-	V
4	0100	-	1.95	-	V
5	0101	-	2.02	-	V
6	0110	-	2.10	-	V
7	0111	-	2.18	-	V
8	1000	-	2.32	-	V
9	1001	-	2.43	-	V
10	1010	-	2.56	-	V
11	1011	-	2.69	-	V
12	1100	-	2.90	-	V
13	1101	-	3.08	-	V
14	1110	-	3.33	-	V
15	1111	-	3.57	-	V

Table 10.4: Voltage Output Steps

Output Step	CUR_SET[3:0]	Typ	Units
0	0000	0.200	mA
1	0001	0.280	mA
2	0010	0.340	mA
3	0011	0.420	mA
4	0100	0.480	mA
5	0101	0.530	mA
6	0110	0.610	mA
7	0111	0.670	mA
8	1000	0.750	mA
9	1001	0.810	mA
10	1010	0.860	mA
11	1011	0.950	mA
12	1100	1.000	mA
13	1101	1.090	mA
14	1110	1.140	mA
15	1111	1.230	mA

Table 10.5: Current Output Steps

Note:

For BAT_P, the PSRR at 100Hz to 22kHz, with >300mV supply headroom, decoupling capacitor of 1.1µF, is typically 58.9dB and worst case 53.4dB.

For VDD_AUDIO, the PSRR at 100Hz to 22kHz, decoupling capacitor of 1.1µF, is typically 88dB and worst case 60dB.

10.6 Line Input

If the input analogue gain is set to less than 24dB, BC6140 QFN automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting. Figure 10.4 and Figure 10.5 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

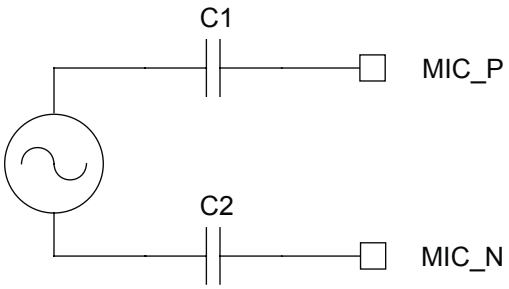

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Figure 10.4: Differential Input

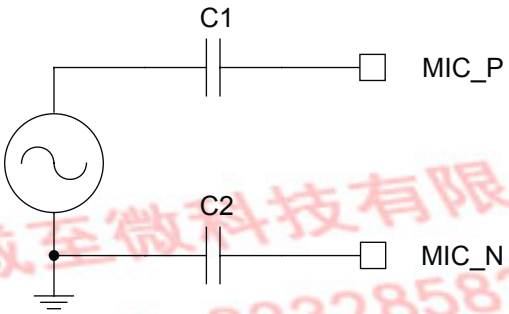

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Figure 10.5: Single-ended Input

10.7 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit comprises a DAC with gain setting and class AB output stage amplifier. The output is available as a differential signal between SPKR_N and SPKR_P, as Figure 10.6 shows.

The output stage is capable of driving a speaker directly when its impedance is at least 8Ω and an external regulator is used, but this will be at a reduced output swing.

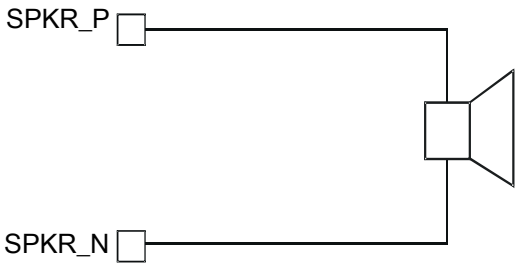

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Figure 10.6: Speaker Output

A 3-bit programmable resistive divider controls the analogue gain of the output stage, which sets the gain in steps of approximately 3dB.

10.8 Integrated Digital Filter

BC6140 QFN has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2 stage, second order IIR and is used for functions such as custom wind noise rejection. The filter also has optional DC blocking.

The filter has 10 configuration words used as follows:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format `XX.XXXXXXXXXX`

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

`01.1111111111` = most positive number, close to `2`

`01.0000000000` = `1`

`00.0000000000` = `0`

`11.0000000000` = `-1`

`10.0000000000` = `-2`, most negative number

Equation 10.1 shows the equation for the IIR filter. Equation 10.2 shows the equation for when the DC blocking is enabled.

The filter can be configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the order shown below:

`0` : Gain

`1` : b_{01}

`2` : b_{02}

`3` : a_{01}

`4` : a_{02}

`5` : b_{11}

`6` : b_{12}

`7` : a_{11}

`8` : a_{12}

`9` : DC Block (1 = enable, 0 = disable)

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01}\, z^{-1} + b_{02}\, z^{-2})}{(1 + a_{01}\, z^{-1} + a_{02}\, z^{-2})} \times \frac{(1 + b_{11}\, z^{-1} + b_{12}\, z^{-2})}{(1 + a_{11}\, z^{-1} + a_{12}\, z^{-2})}$$

Equation 10.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 10.2: IIR Filter plus DC Blocking Transfer Function, $H_{DC}(z)$

10.8.1 Integrated Digital Filter Configuration

The behaviour of the integrated digital IIR filter described in Section 10.8, is configurable through 12 values stored in PSKEY_USR29:

- 10-words for the IIR filter parameters in Section 10.8
- 1-word for the audio energy estimation threshold
- 1-word for the gain to be applied when the audio energy estimation is above the threshold

Adjusting these values configures the IIR filter for different functions:

- Echo reduction, see Section 10.8.2
- Noise reduction (wind noise filter), see Section 10.8.3

Note:

The IIR filter is switched off at initialisation.

10.8.2 Echo Reduction

The echo reduction feature on BC6140 QFN uses the integrated digital IIR filter in Section 10.8.

In order to implement the echo reduction feature the energy estimation of the SCO connections is constantly monitored. When the energy estimation goes above a given threshold, the IIR filter is switched on. When the energy estimation goes below a given threshold, the IIR filter is switched off. Additionally, the echo reduction gain is applied to the filter.

10.8.3 Noise Reduction

The noise reduction feature on BC6140 QFN uses the integrated digital IIR filter in Section 10.8 to create a wind noise filter.

The wind noise filter is basically a high-pass filter that is always on. To achieve this:

- The filter threshold is set to 0
- The filter echo reduction gain is set to 0
- The filter coefficients are left at their default values

However, it is possible to calculate values for a custom configuration using the filter equation, see Equation 10.1 and Equation 10.2.

10.9 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BC6140 QFN codec contains side tone circuitry to do this. The side tone hardware is configured through the following PS Keys:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

11 Power Control and Regulation

BC6140 QFN contains 3 regulators:

- A switch-mode regulator, used to generate a 1.5V rail
- A low-voltage regulator which can generate an optional 1.5V rail
- A high-voltage linear regulator used to generate a 1.9V rail for powering the EEPROM

Various configurations for power control and regulation with BC6140 QFN are available, but a typical configuration is shown in Figure 11.1. This configuration has the switch-mode regulator generating a 1.5V supply rail, and the high-voltage linear regulator creating a 1.9V supply rail.

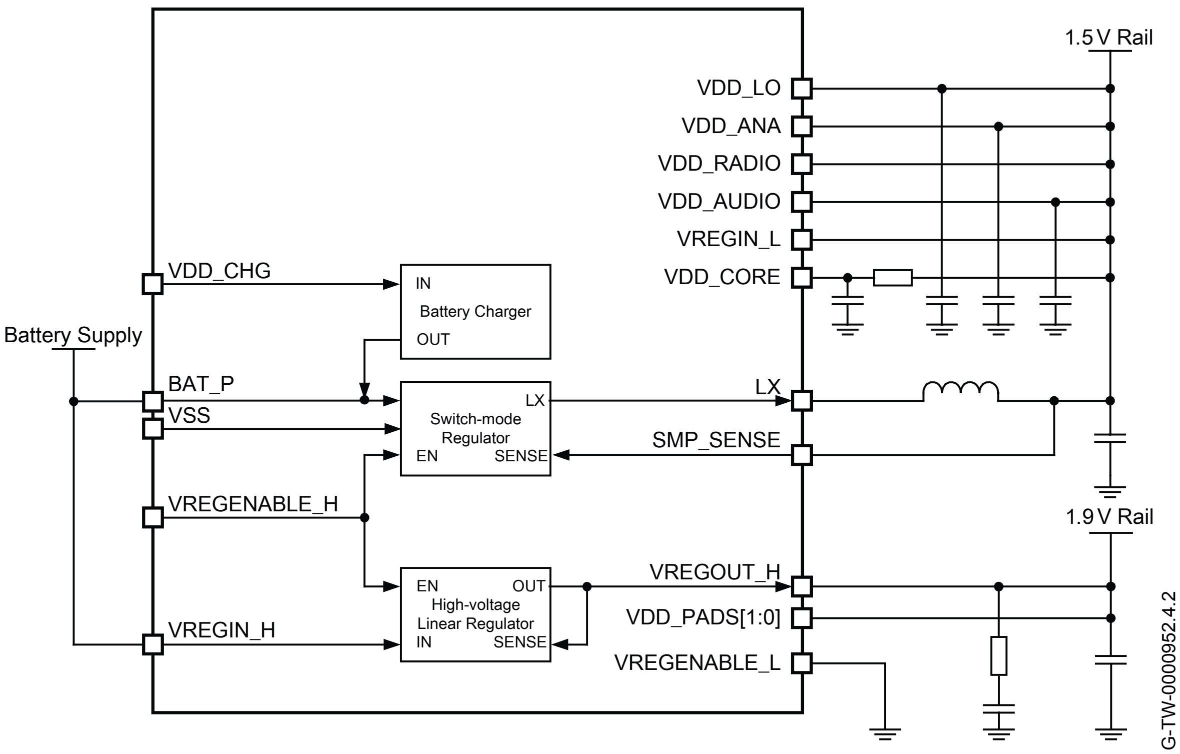

Figure 11.1: Voltage Regulator Configuration

11.1 Power Sequencing

The 1.5V supply rails are VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PADS[1:0].

The sequence of powering the 1.5V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.5V supply rails, all digital I/Os will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_AUDIO, VDD_LO and VDD_RADIO can connect directly to a 1.5V supply.

A simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The digital I/O supply rails are connected either together or independently to an appropriate voltage rail. Decoupling of the digital I/O supply rails is recommended.

11.2 External Voltage Source

If any of the supply rails for BC6140 QFN are supplied from an external voltage source, rather than one of the internal voltage regulators, CSR recommends that VDD_AUDIO, VDD_LO and VDD_RADIO should have less than 10mV rms noise levels between 0 and 10MHz. Also avoid single tone frequencies.

The transient response of any external regulator used should match or be better than the internal regulator available on BC6140 QFN. For more information, refer to regulator characteristics in Section 13. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

11.3 Switch-mode Regulator

CSR recommends the on-chip switch-mode regulator to power the 1.5V supply rail.

An external LC filter circuit of a low-resistance series inductor, L1 (22µH), followed by a low ESR shunt capacitor, C1 (4.7µF), is required between the LX terminal and the 1.5V supply rail. A connection between the 1.5V supply rail and the SMP_SENSE pin is required.

A 2.2µF decoupling capacitor is required between BAT_P and VSS.

To maintain high-efficiency power conversion and low supply ripple, it is essential that the series resistance of tracks between the BAT_P and VSS terminals, the filter and decoupling components, and the external voltage source are minimised.

The switch-mode regulator is enabled by either:

- VREGENABLE_H pin
- BC6140 QFN device firmware
- BC6140 QFN battery charger

The switch-mode regulator switches into a low-power pulse skipping mode when the device is sent into deep sleep mode, or in reset.

When the switch-mode regulator is not required the terminals BAT_P and LX must be grounded or left unconnected.

11.4 High-voltage Linear Regulator

The 1.9V high-voltage linear regulator provides power for an external EEPROM. The external EEPROM stores PS Key and configuration information, see Section 9.3. CSR does not recommend using the high-voltage linear regulator to power any additional circuitry.

A smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, should be connected to the output of the high-voltage linear regulator, VREGOUT_H. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The high-voltage linear regulator is enabled by either:

- VREGENABLE_H pin
- BC6140 QFN device firmware
- BC6140 QFN battery charger

The regulator is switched into a low-power mode when the device is in deep sleep mode, or in reset.

11.5 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.5V supply rail. Its output is connected internally to VDD_ANA, and can be connected externally to the other 1.5V power inputs.

If the low-voltage linear regulator is used, connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by either:

- VREGENABLE_L pin
- BC6140 QFN device firmware
- BC6140 QFN battery charger

The low-voltage linear regulator switches into a low power mode when the device is in deep sleep mode, or in reset.

When the low-voltage linear regulator is not used, either leave the terminal VREGIN_L unconnected, or tie it to VDD_ANA.

11.6 Voltage Regulator Enable Pins

The voltage regulator enable pins, VREGENABLE_H and VREGENABLE_L, are used to enable the BC6140 QFN device if the on-chip regulators are being used. Table 11.1 shows the enable pin responsible for each voltage regulator.

Enable Pin	Regulator
VREGENABLE_H	High-voltage Linear Regulator and Switch-mode Regulator
VREGENABLE_L	Low-voltage Linear Regulator

Table 11.1: BC6140 QFN Voltage Regulator Enable Pins

The voltage regulator enable pins are active high, with weak pull-downs.

BC6140 QFN boots-up when the voltage regulator enable pins are pulled high, enabling the appropriate regulators. The firmware then latches the regulators on and the voltage regulator enable pins may then be released.

The status of the VREGENABLE_H pin is available to firmware through an internal connection. VREGENABLE_H also works as an input line.

11.7 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, BAT_P, with the switch-mode regulator. However it may be used in conjunction with either of the high-voltage regulators on the device.

The constant current level can be varied to allow charging of different capacity batteries.

The charger enters various states of operation as it charges a battery, as listed below. A full operational description is in *BlueCore5 Charger Description and Calibration Procedure Application Note*:

- Off : entered when charger disconnected.
- Trickle charge: entered when battery is below 2.9V. The battery is charged at a nominal 4.5mA. This mode is for the safe charge of deeply discharged cells.
- Fast charge constant current: entered when battery is above 2.9V. The charger enters the main fast charge mode. This mode charges the battery at the selected constant current, I_{chgset}.
- Fast charge constant voltage: entered when battery has reached a selected voltage, V_{float}. The charger switches mode to maintain the cell voltage at the V_{float} voltage by adjusting the charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place. The battery voltage is continuously monitored and if it drops by more than 150mV below the V_{float} voltage the charger will re-enter the fast charge constant current mode to keep the battery fully charged.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger operates and an LED connected to the terminal LED[0] illuminates. By default, until the firmware is running, the LED pulses at a low-duty cycle to minimise current consumption.

The battery charger circuitry auto-detects the presence of a power source, allowing the firmware to detect, using an internal status bit, when the charger is powered. Therefore when the charger supply is not connected to VDD_CHG, the terminal must be left open-circuit. The VDD_CHG pin when not connected must be allowed to float and not pulled to a power rail. When the battery charger is not enabled this pin may float to a low undefined voltage. Any DC connection increases current consumption of the device. Capacitive components may be connected such as diodes, FETs and ESD protection.

The battery charger is designed to operate with a permanently connected battery. If the application enables the charger input to be connected while the battery is disconnected, then the BAT_P pin voltage may become unstable. This in turn may cause damage to the internal switch-mode regulator. Connecting a 470µF capacitor to BAT_P limits these oscillations so preventing damage.

11.8 LED Drivers

BC6140 QFN includes 2 pads dedicated to driving LED indicators. Both terminals can be controlled by firmware, while LED[0] can also be set by the battery charger.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor.

CSR recommends that the LED pad, LED[0] or LED[1] pins, operate with a pad voltage below 0.5V. In this case, the pad is like a resistor, R_{ON}. The resistance together with the external series resistor sets the current, I_{LED}, in the LED. The current is also dependent on the external voltage, VDD, as Figure 11.2 shows.

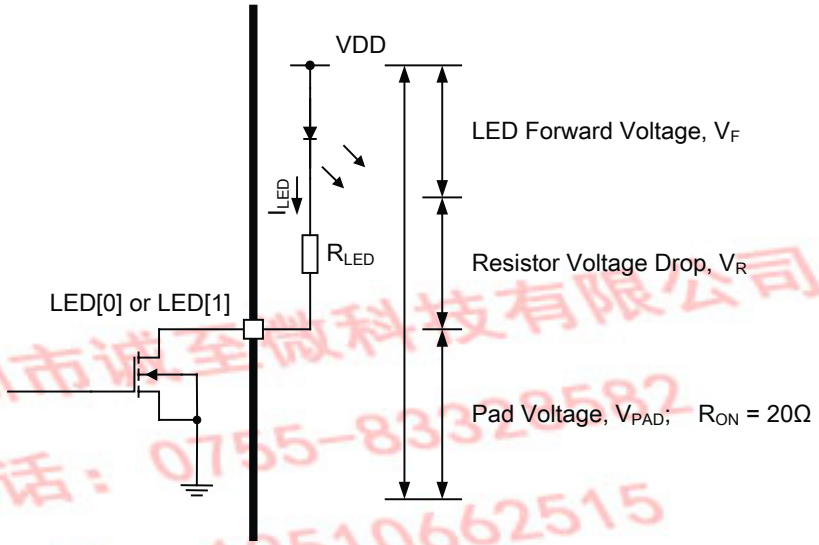

Figure 11.2: LED Equivalent Circuit

From Figure 11.2 it is possible to derive Equation 11.1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} can be calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 11.1: LED Current

For the LED[0] or LED[1] pad to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 11.2 also applies.

$$VDD = V_F + V_R + V_{PAD}$$

Equation 11.2: LED PAD Voltage

Note:

The LED current adds to the overall current, so conservative selection of the LEDs will extend battery life.

11.9 Reset, RST#

BC6140 QFN can be reset from several sources:

- RST# pin
- Power-on reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. CSR recommends that RST# be applied for a period greater than 5ms.

The power-on reset typically occurs when the VDD_CORE supply falls below 1.25V and is released when VDD_CORE rises above typically 1.30V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tristate. Following a reset, BC6140 QFN assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BC6140 QFN is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BC6140 QFN free runs, again at a safe frequency.

11.9.1 Digital Pin States on Reset

Table 11.2 shows the pin states of BC6140 QFN on reset. PU and PD default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
UART_RX	Digital input with PD	PD	PD
UART_TX	Digital bidirectional with PU	PD	PD
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital bidirectional with PD	PD	PD
SPI_CS#	Digital bidirectional with PD	PD	PD
SPI_MISO	Digital tristate output with PD	PD	PD
SPI_DEBUG_EN	Digital input with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with strong PD	PD	PD
PIO[11,3:0] PIO[8:6]	Digital bidirectional with PU/ PD	PD	PD

Table 11.2: Pin States on Reset

11.9.2 Status after Reset

The status of BC6140 QFN after a reset is:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

12 Example Application Schematic

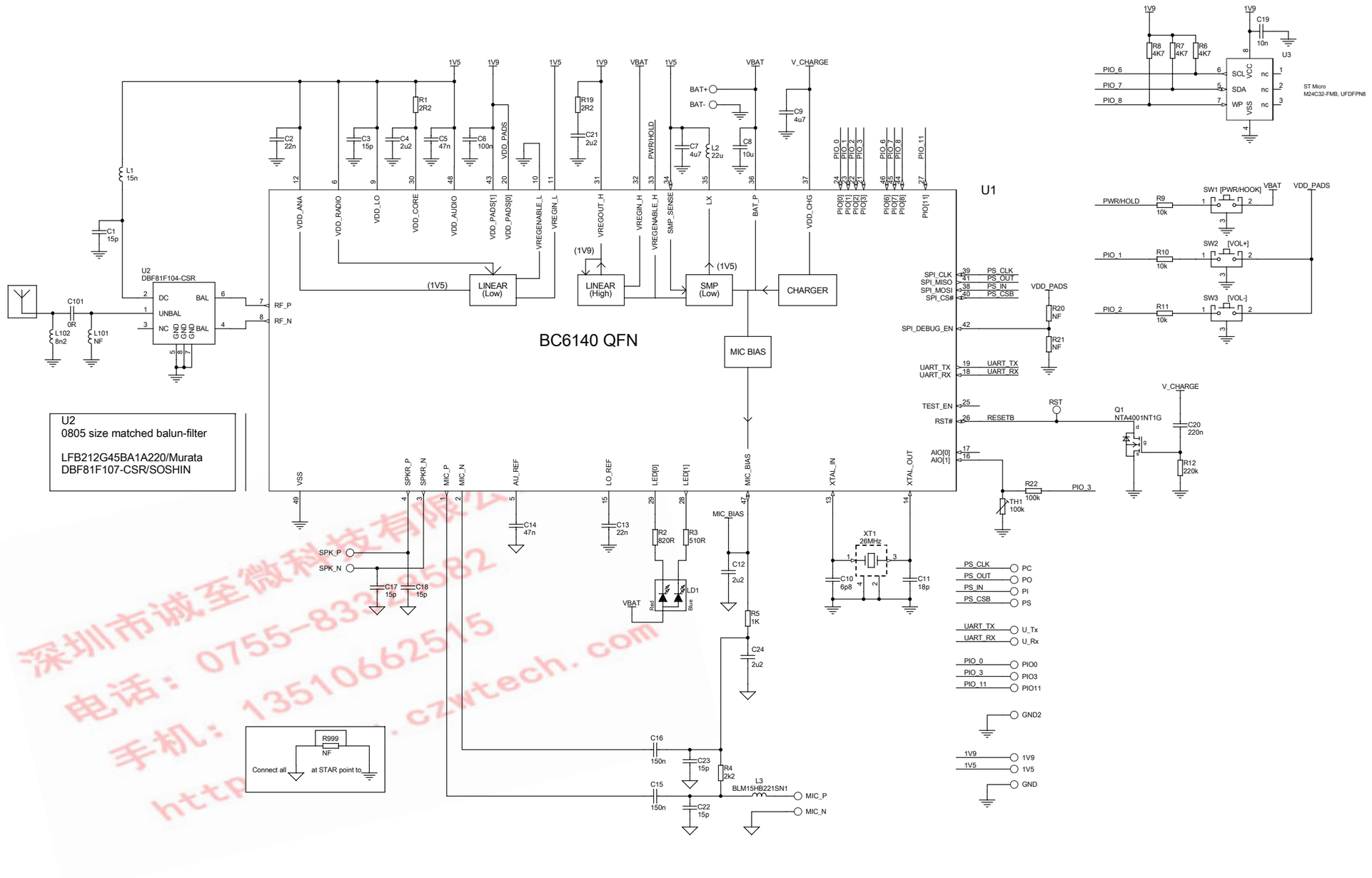

Figure 12.1: Example Application Schematic

G-TW-0003615.4.2

13 Electrical Characteristics

13.1 ESD Precautions

BC6140 QFN is classified as a JESD22-A114 class 2, JESD22-A115 class B product. Apply ESD static handling precautions during manufacturing.

13.2 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	105	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	-0.4	1.65	V
I/O Voltage	VDD_PADS[1:0]	-0.4	3.6	V
Supply Voltage	VREGIN_L	-0.4	2.7	V
	VREGIN_H, VREGENABLE_H and VREGENABLE_L	-0.4	4.9	V
	BAT_P	-0.4	4.4	V
	LED[1:0]	-0.4	4.4	V
	VDD_CHG	-0.4	6.5	V
Other Terminal Voltages		VSS - 0.4	VDD + 0.4	V

13.3 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range[a]		-20	20	70	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	1.42	1.50	1.57	V
I/O Supply Voltage	VDD_PADS[1:0]	1.7	3.3	3.6	V

[a] For radio performance over temperature refer to *BC6140 QFN Performance Specification*.

13.4 Input/Output Terminal Characteristics

Note:

For all I/O Terminal Characteristics:

- VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO at 1.5V unless shown otherwise.
- VDD_PADS[1:0] at 3.3V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

13.4.1 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.7	-	4.9	V
Output voltage (I_{load} = 25mA / VREGIN_H = 3.0V)	1.80	1.90	2.05	V
Temperature coefficient	-300	0	300	ppm/°C
Output Noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 25mA), ΔV_{out}	-	-	5	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	25	mA
Minimum load current	5	-	-	µA
Quiescent current (excluding load, I_{load} < 1mA)	30	50	60	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	11	15	21	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

[b] Frequency range 100Hz to 100kHz.

[c] 1mA to 25mA pulsed load.

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset.

13.4.2 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.7	-	4.4	V
Output voltage (I_{load} = 70mA)	1.42	1.50	1.57	V
Temperature coefficient	-250	-	250	ppm/°C
Normal Operation				
Output ripple	-	-	10	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	200	-	-	mA
Conversion efficiency (I_{load} = 70mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	30	50	80	mA
Low-power Mode [d]				
Output ripple	-	-	1	mV rms
Transient settling time[e]	-	-	700	µs
Maximum load current	5	-	-	mA
Minimum load current	1	-	-	µA
Conversion efficiency (I_{load} = 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz

[a] For step changes in load of 30 to 80mA and 80 to 30mA.

[b] Locked to crystal frequency.

[c] Current is limited on start-up to prevent excessive stored energy in the filter inductor.

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset.

[e] 100µA to 1mA pulsed load.

[f] Defines minimum period between pulses. Pulses are skipped at low current loads.

Note:

The external inductor used with the switch-mode regulator must have an ESR in the range 0.3Ω to 0.7Ω:

- Low ESR < 0.3Ω causes instability.
- High ESR > 0.7Ω derates the maximum current.

13.4.3 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.80	2.00	2.70	V
Output voltage (I_{load} = 70mA / VREGIN_L = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 90mA), ΔV_{out}	-	-	5	mV
Load regulation (100µA < I_{load} < 115mA), ΔV_{out}	-	-	25	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	115	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

[b] Frequency range 100Hz to 100kHz.

[c] 1mA to 115mA pulsed load.

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset.

13.4.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	-	6.5	V

Charging Mode (BAT_P rising to 4.2V)		Min	Typ	Max	Unit
Supply current[a]		-	4.5	6	mA
Battery trickle charge current[b] [c]		-	4	-	mA
Maximum battery fast charge current (I-CTRL = 15)[c] [d]	Headroom[e] > 0.7V	-	150	-	mA
	Headroom = 0.3V	-	120	-	mA
Minimum battery fast charge current (I-CTRL = 0)[c] [d]	Headroom > 0.7V	-	40	-	mA
	Headroom = 0.3V	-	35	-	mA
Fast charge step size (I-CTRL = 0 to 15)	Spread ±17%	-	6.3	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), V_{FLOAT} [f]		4.17	4.2	4.23	V
Float voltage trim step size[f]		-	50	-	mV
Battery charge termination current, % of fast charge current		5	10	20	%

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] BAT_P < Float voltage

[c] Charge current can be set in 16 equally spaced steps.

[d] Trickle charge threshold < BAT_P < Float voltage

[e] Where headroom = VDD_CHG - BAT_P

[f] Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

Standby Mode (BAT_P falling from 4.2V)	Min	Typ	Max	Unit
Supply current[a]	-	1.5	2	mA
Battery current	-	-5	-	µA
Battery recharge hysteresis[b]	100	-	200	mV

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

Shutdown Mode (VDD_CHG too low or disabled by firmware)		Min	Typ	Max	Unit
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.90	-	V
	VDD_CHG falling	-	3.70	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V
Supply current		-	1.5	2	mA
Battery current		-1	-	0	µA

13.4.5 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

13.4.6 Regulator Enable

Switching Threshold	Min	Typ	Max	Unit
VREGENABLE_H				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V
VREGENABLE_L				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V

13.4.7 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
VDD_{PRE}	Pre-driver supply voltage	1.4	1.5	1.6	V
VDD I/O supply voltage (post-driver)	Full spec.	3.0	3.3	3.6	V
	Reduced spec.	1.7	-	3.0	V

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-0.3	-	0.25 x VDD	V
V_{IH} input logic level high	0.625 x VDD	-	VDD + 0.3	V
$V_{SCHMITT}$ Schmitt voltage	0.25 x VDD	-	0.625 x VDD	V

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 4.0mA	0	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD	-	VDD	V

Input and Tristate Currents	Min	Typ	Max	Unit
I_i input leakage current at V_{in} = VDD or 0V	-100	0	100	nA
I_{oz} tristate output leakage current at V_o = VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	-0.2	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

Resistive Strength	Min	Typ	Max	Unit
R_{puw} weak pull-up strength at VDD - 0.2V	0.5	-	2	MΩ
R_{pdw} weak pull-down strength at 0.2V	0.5	-	2	MΩ
R_{pus} strong pull-up strength at VDD - 0.2V	10	-	50	kΩ
R_{pds} strong pull-down strength at 0.2V	10	-	50	kΩ

13.4.8 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Off current		-	1	2	µA
On resistance	V_{PAD} < 0.5V	-	20	33	Ω
On resistance, pad enabled by battery charger	V_{PAD} < 0.5V	-	20	50	Ω

13.4.9 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_ANA/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

13.4.10 Mono Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	32	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mV$_{pk-pk}$ input	F_{sample}				
		8kHz	-	79	-	dB
		11.025kHz	-	77	-	dB
		16kHz	-	76	-	dB
		22.050kHz	-	76	-	dB
		32kHz	-	75	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-3	-3	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

13.4.11 Mono Codec: Digital to Analogue Converter

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Output Sample Rate, F_{sample}	-		8	-	32	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.01% 0dBFS signal Load = 100kΩ	F_{sample}				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	dB
		16kHz	-	95	-	dB
		22.050kHz	-	95	-	dB
		32kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full-scale swing (differential)			-	750	-	mV rms
Allowed Load		Resistive	16(8)	-	O.C.	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

13.4.12 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	16	26	26	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

14 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		HV3	30	9.46	mA
Slave	eSCO		EV3	30	10.82	mA
Slave	eSCO		2EV3	60	7.71	mA
Slave	eSCO		2EV3	30	10.66	mA
Slave	SCO	1-mic CVC	HV3	30	11.42	mA
Slave	eSCO	1-mic CVC	2EV3	60	9.65	mA
Slave	eSCO	1-mic CVC	2EV3	30	12.63	mA
Slave	ACL	Sniff = 100ms	-	-	0.87	mA
Slave	ACL	Sniff = 500ms	-	-	0.37	mA
Slave	ACL	Sniff = 1280ms	-	-	0.29	mA
Master	SCO		HV3	30	9.55	mA
Master	eSCO		EV3	30	9.89	mA
Master	eSCO		2EV3	60	7.25	mA
Master	eSCO		2EV3	30	9.44	mA
Master	SCO	1-mic CVC	HV3	30	11.53	mA
Master	eSCO	1-mic CVC	2EV3	60	9.19	mA
Master	eSCO	1-mic CVC	2EV3	30	11.39	mA
Master	ACL	Sniff = 100ms	-	-	0.96	mA
Master	ACL	Sniff = 500ms	-	-	0.38	mA
Master	ACL	Sniff = 1280ms	-	-	0.27	mA

Note:

Current consumption values are taken with:

- BAT_P pin for switch-mode regulator = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected, with internal microphone bias circuit set to minimum current level
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected

15 CSR Green Semiconductor Products and RoHS Compliance

15.1 RoHS Statement

BC6140 QFN where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

15.1.1 List of Restricted Materials

BC6140 QFN is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

In addition, the following substances are not intentionally added to BC6140 QFN devices:

- Halogenated flame retardant
- Antinomy (Sb) and Compounds, including Antimony Trioxide flame retardant
- Polybrominated Diphenyl and Biphenyl Oxides
- Tetrabromobisphenol-A bis (2,3-dibromopropylether)
- Asbestos or Asbestos compounds
- Azo compounds
- Organic tin compounds
- Mirex
- Polychlorinated napthelenes
- Polychlorinated terphenyls
- Polychlorinated biphenyls
- Polychlorinated/Short chain chlorinated paraffins
- Polyvinyl Chloride (PVC) and PVC blends
- Formaldehyde
- Arsenic and compounds (except as a semiconductor dopant)
- Beryllium and its compounds
- Ethylene Glycol Monomethyl Ether or its acetate
- Ethylene Glycol Monoethyl Ether or its acetate
- Halogenated dioxins and furans
- Persistent Organic Pollutants (POP), including Perfluorooctane sulphonates
- Red phosphorous
- Ozone Depleting Chemicals (Class I and II): Chlorofluorocarbons (CFC) and Halons
- Radioactive substances

For further information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products.*

16 BC6140 QFN Software Stack

BC6140 QFN is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU.

The BC6140 QFN software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC MCU and an external host processor, if any. The upper layers of the Bluetooth stack, above the HCI, can be run either on-chip or on the host processor.

16.1 BC6140 QFN Low-cost Mono DSP Headset Solution Development Kit

CSR's BC6140 QFN low-cost mono DSP headset solution development kit for BC6140 QFN, order code DK-BC-6140-1A, includes a headset demonstrator board, form-factor representative example design, music and voice dongle and necessary interface adapters and cables. In conjunction with the BlueVox Configurator tool and other supporting utilities the development kit provides the best environment for designing a mono headset solution with BC6140 QFN.

16.2 BC6140 QFN Low-cost Mono DSP Headset Solution

- The CSR mono headset ROM software supports HFP v1.5 and HSP v1.1. Advanced features in these specifications are supported, including three-way calling.
- Bluetooth v2.1 + EDR specification is supported in the ROM software including Secure Simple Pairing, greatly simplifying the pairing process.
- Proximity Pairing (headset initiated pairing) for greatly simplifying the out-of-box pairing process, for more information see Section 16.5.
- For connection to more than one mobile phone Advanced Multipoint is supported. This allows a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This is supported with a minimal impact on power consumption and can be easily configured.
- The BC6140 QFN low-cost mono DSP headset solution includes noise reduction hardware controlled by the on-chip MCU. This improves the clarity of the speech in noisy environments.
- Most of the CSR mono headset ROM software features can be configured on the BC6140 QFN using the BlueVox Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions. The tool can be used to read and write headset configurations directly to the EEPROM or alternatively to a PSR file. Configurable headset features include:
  - Bluetooth v2.1 + EDR specification features
  - Reconnection policies, e.g. reconnect on power on
  - Audio features, including default volumes
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for Last Number redial
  - LED indications for states, e.g. headset connected, and events, e.g. power on
  - Indication tones for events and ringtones
  - HFP v1.5 supported features
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
  - Advanced Multipoint settings
- The BC6140 QFN low-cost mono DSP headset solution has undergone extensive interoperability testing to ensure that it will work with the majority of phones on the market

16.3 Advanced Multipoint Support

Advanced Multipoint allows the connection of 2 devices to BC6140 QFN at the same time. For example, this could be either 2 phones connected to a BC6140 QFN headset, or a phone and a VoIP dongle connected to a headset.

The BC6140 QFN low-cost mono DSP headset solution:

- Supports a maximum of 2 connections (either HFP or HSP)
- Allows multiple calls to be handled from both devices at the same time
- During a call from 1 device, all headset buttons work as in the standard use case with one device connected
- During multiple calls (1 on each device), all headset buttons work as in the standard use case for a single AG with multiple calls in progress (three-way calling)
- This implementation is easy to use with negligible effect on power consumption

16.4 Programmable Audio Prompts

Figure 16.1 shows that users can configure and load pre-programmed audio prompts from an external EEPROM. The prompts provide a mechanism for higher quality audio indications to replace standard tone indications. In this way, a programmable audio prompt can be assigned to any user event in place of a standard tone.

Programmable audio prompts can contain either voice prompts to indicate that events have occurred or they can provide user defined higher quality ring tones / indications, e.g. custom power on/off tones. The prompts are stored in the same EEPROM as used for standard PS Keys, see Section 9.3. In this way, a larger EEPROM is required for programmable audio prompts. EEPROMs up to 512Kb are supported for use in this way. An EEPROM of 512Kb allows approximately 15 seconds of audio to be stored.

The content of the programmable audio prompts can be generated from standard WAV audio files using the BlueVOX Configurator tool. The tool also allows the configuration of which prompts are assigned to which user events.

Section 9.3 describes the I^2C interface to the external EEPROM.

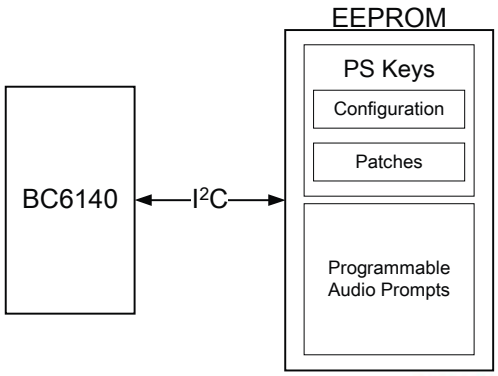

Figure 16.1: Programmable Audio Prompts in External I^2C EEPROM

16.5 Proximity Pairing

Proximity Pairing is headset intiated pairing and it simplifies the out-of-box pairing process. Proximity Pairing allows the headset to find the closest discoverable phone. The headset then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus in order to pair with the new headset.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the headset pairing is with a PIN code
- For a Bluetooth v2.1 phone the headset pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. In order to do this, the headset finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and is defined as the closest device, the headset will then attempt to pair with and connect to this device.

16.5.1 Proximity Pairing Configuration

Proximity Pairing is configurable using the BlueVox Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions.

17 Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
BC6140 QFN Low-cost Mono DSP Headset Solution	QFN 48-lead (Pb free)	7 x 7 x 0.9mm, 0.5mm pitch	Tape and reel	BC6140A02-IQQB-R

Note:

BC6140 QFN is a ROM-based device where the product code has the form BC6140Axx. Axx is the specific ROM-variant, A02 is the ROM-variant for BC6140 QFN Low-cost Mono DSP Headset Solution.

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts.

17.1 BC6140 QFN Low-cost Mono DSP Headset Solution Development Kit Ordering Information

Description	Order Number
BC6140 QFN Low-cost Mono DSP Headset Solution Development Kit, including headset example design	DK-BC-6140-1A

18 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

18.1 Tape Orientation

Figure 18.1 shows the BC6140 QFN packing tape orientation.

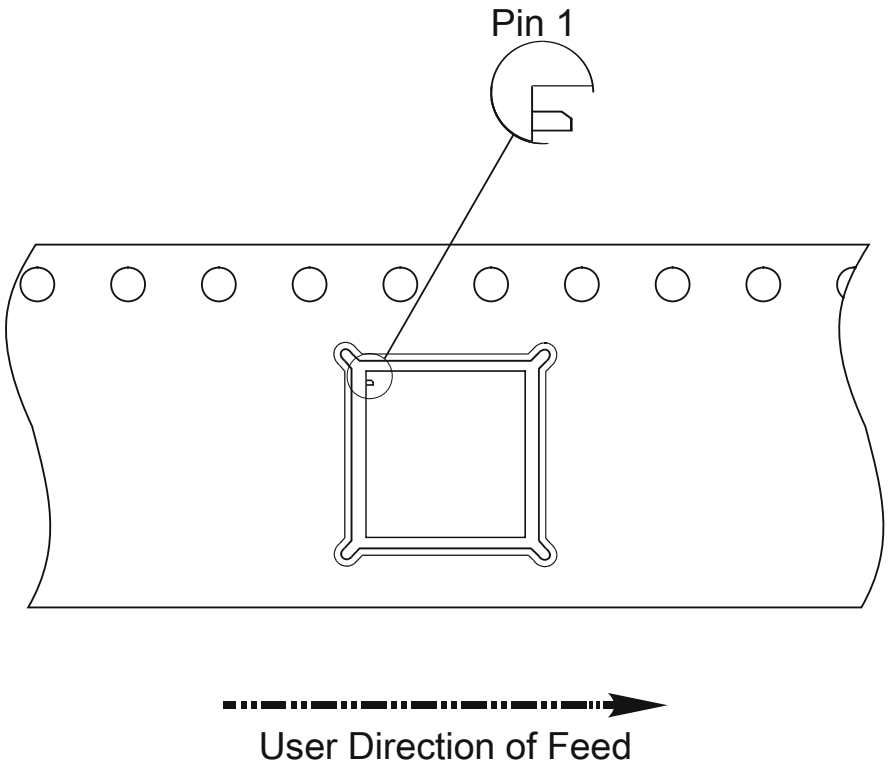

Figure 18.1: Tape Orientation

G-TW-0002812.2.2

18.2 Tape Dimensions

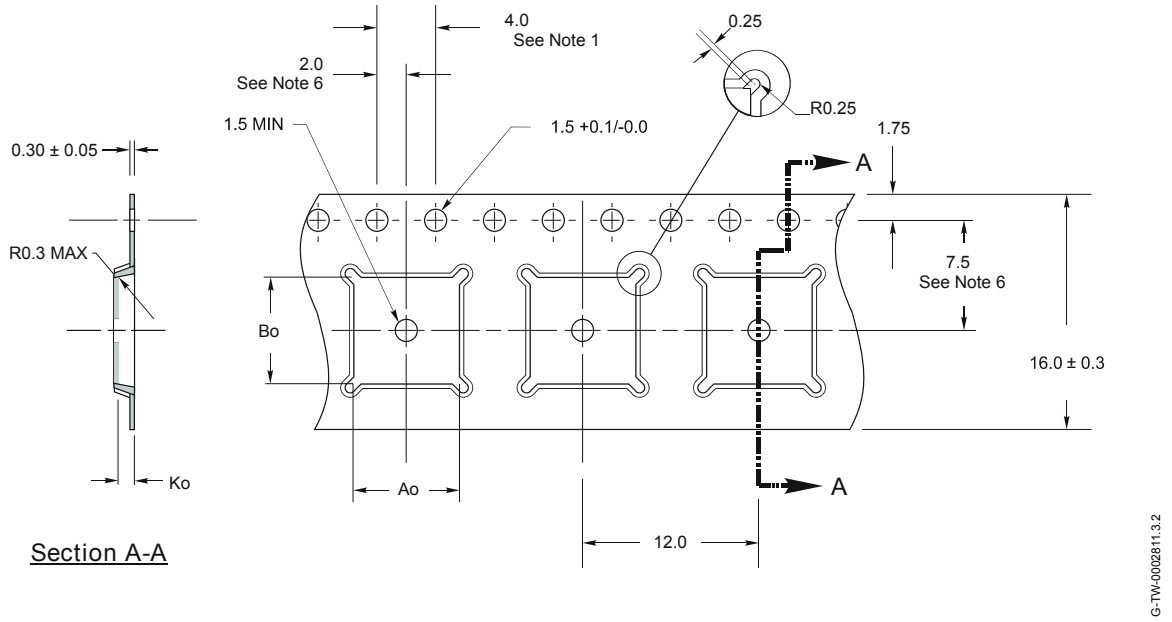

Figure 18.2: Tape Dimensions

A_0	B_0	K_0	Unit	Notes
7.25	7.25	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

18.3 Reel Information

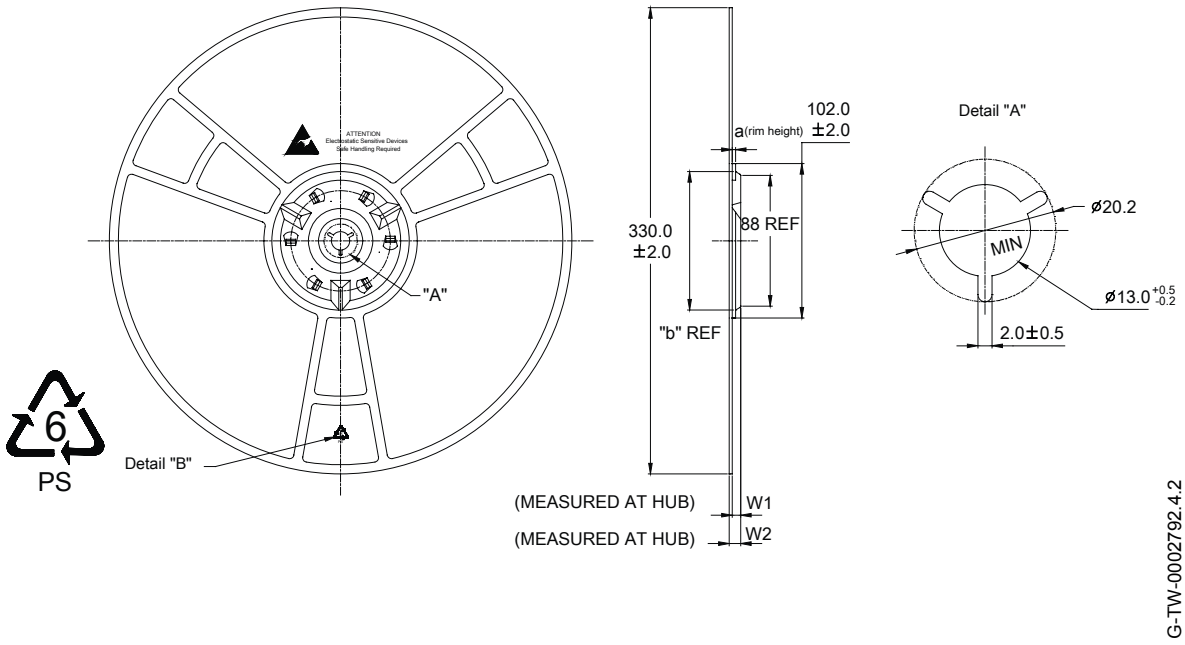

Figure 18.3: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
7 x 7 x 0.9mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

18.4 Moisture Sensitivity Level

BC6140 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

19 Document References

Document	Reference, Date
BlueCore5 Charger Description and Calibration Procedure Application Note	CS-113282-ANP, 2007
BC6140 QFN Performance Specification	CS-124326-SP, 2009
Core Specification of the Bluetooth System	v2.1 + EDR, 2007
Enhancing Microphone Bias Performance in Headset Designs using BlueVox2 Application Note	CS-121678-ANP, 2008
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST, 2007
IC Packing and Labelling Specification	CS-112584-SPP, 2007
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008P, 2004
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 2006
Typical Solder Reflow Profile for Lead-free Device	CS-116434-ANP, 2007

Terms and Definitions

Term	Definition
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AG	Audio Gateway
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ALU	Arithmetic logic unit
B/W	BandWidth
BIST	Built-In Self-Test
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CVC	Clear Voice Capture
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor
DUT	Device Under Test
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
HCI	Host Controller Interface
HFP	Hands-Free Profile
HSP	HeadSet Profile
I^2C	Inter-Integrated Circuit Interface
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency

Term	Definition
IIR	Infinite Impulse Response (filter)
INL	Integral Non Linearity (ADC accuracy parameter)
IPC	See www.ipc.org
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression, and file compression / decompression
Kb	Kilobit
LC	An inductor (L) and capacitor (C) network
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
MAC	Medium Access Control
MAC	Multiplier and ACcumulator
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out
MMU	Memory Management Unit
NSMD	Non Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pull-down
PIN	Personal Identification Number
PIO	Programmable Input/Output
plc	Public Limited Company
ppm	parts per million
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PU	Pull-up
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RC	Resistor Capacitor
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented
SIG	(Bluetooth) Special Interest Group
SNR	Signal-to-Noise Ratio

Term	Definition
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
VoIP	Voice over Internet Protocol
XTAL	Crystal