Features

- Single-chip Bluetooth® mono headset solution
- Low power consumption: up to 12 hours talk time from a 120mAh battery
- Support for Secure Simple Pairing
- Proximity Pairing (headset initiated pairing)
- Best-in-class Bluetooth radio with 5.5dBm transmit power and -88dBm receive sensitivity
- Minimum external components
- Configurable mono headset software
- HFP1.5 and HSP1.1 support
- Low-power 1.8V operation
- Integrated switch-mode regulator
- Integrated battery charger with programmable current
- Integrated high-quality mono codec
- 56-lead 8 x 8 x 0.9mm, 0.5mm pitch QFN
- Green (RoHS compliant and no antimony or halogenated flame retardants)
- A complete BC6110 low-cost mono headset solution development kit is available, order code DK-BC-6110-1A

BlueCore®

BC6110™

Fully Qualified Single-chip Bluetooth® v2.1 + EDR System

Production Information

BC6110A14

Issue 2

General Description

BC6110™ is a low-cost fully featured ROM chip solution for mono headsets with low power consumption. It includes a Bluetooth radio, baseband, DAC/ADC, switch-mode power supply and battery charger in a compact QFN package for low-cost designs.

BC6110 supports the latest Bluetooth v2.1 + EDR specification which includes Secure Simple Pairing, greatly simplifying the pairing process, making it even easier for users to get up and running with a Bluetooth headset.

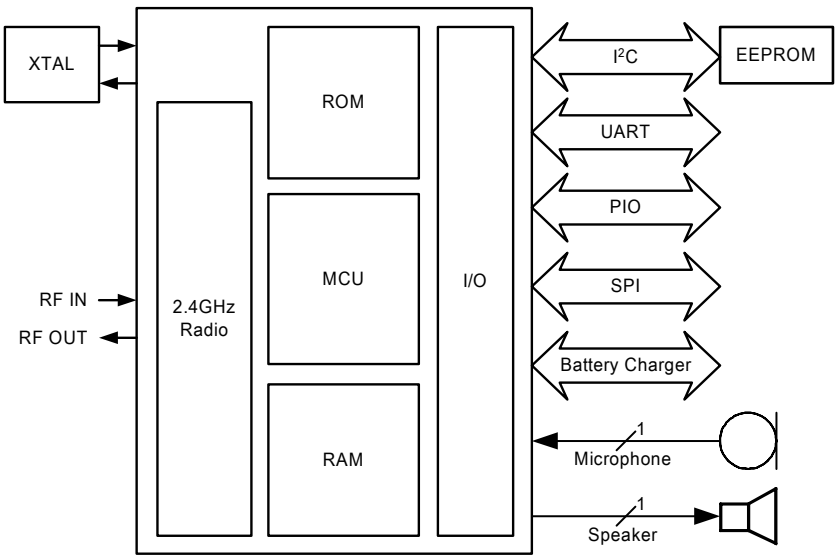
Applications

- Low-cost mono headset solution

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.

BC6110 has been designed to reduce the number of external components required which ensures production costs are minimised.

All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification (all mandatory features).



BC6110 Data Sheet

Document History

Revision	Date	Change Reason
1	10 JUN 09	Original publication of this document.
2	18 JUN 09	Production Information Package dimension updates. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

CSR Green Semiconductor Products and RoHS Compliance

BC6110 devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

BC6110 devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Refer to www.csrsupport.com for compliance and conformance to standards information.

Contents

List of Figures

List of Tables

List of Equations

1 Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Bluetooth v2.1 + EDR specification compliant

Transmitter

- 5.5dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -88dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 8MHz to 32MHz

Audio Codec

- 15-bit resolution, 8kHz sampling frequency
- Digital enhancements to add bass cut, side tone and treble boost
- Analogue enhancements to support single-ended speaker drive capability and reference availability

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 3Mbaud with an optional bypass mode
- I^2C compatible interface used to communicate with an external EEPROM which contains all of the device configuration (PS Keys)

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown and wake up commands with an integrated low power oscillator for ultra low-power Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip linear regulator; 1.8V output from a 2.2 to 4.2V input, can also be used to generate microphone bias
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- Battery charger with programmable current (25 to 100mA) for Lithium Ion/Polymer battery
- LED intensity control for dedicated LED[1] and LED[0] outputs

Baseband and Software

- Internal ROM
- 48KB internal RAM to support EDR. Allows full speed data transfer, mixed voice and data, and full Piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air
- Proximity Pairing (headset initiated pairing)

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Embedded Bluetooth mono headset solution
- Standard HCI

Package Option

- 8 x 8 x 0.9mm, 0.5mm pitch QFN

2 Functional Block Diagram

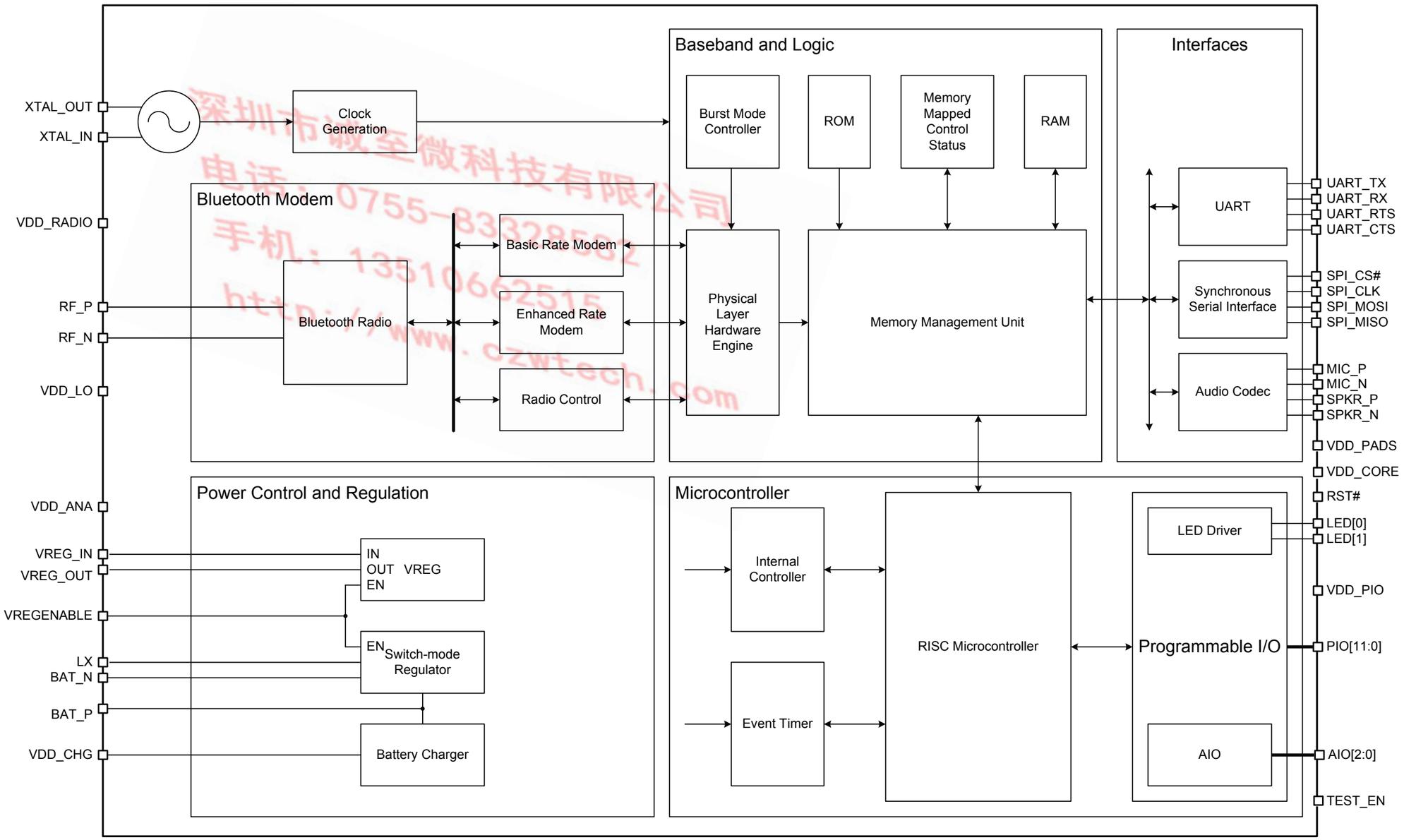


Figure 2.1: Functional Block Diagram

3 Package Information

3.1 Pinout Diagram

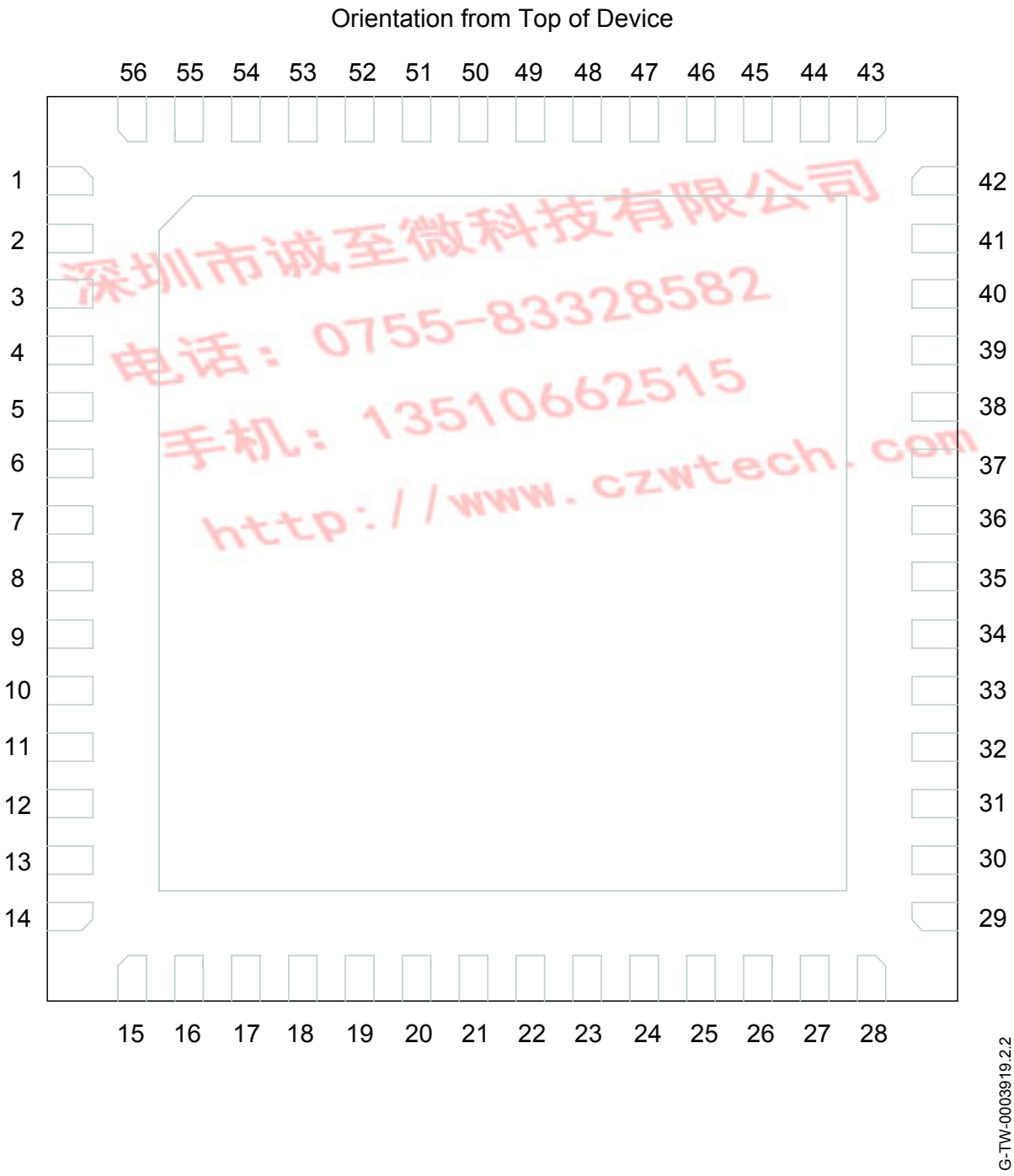


Figure 3.1: Device Pinout

3.2 Device Terminal Functions

Radio	Lead	Pad Type	Description
RF_N	7	Analogue	Transmitter output/switched receiver input
RF_P	6	Analogue	Complement of RF_N

Synthesiser and Oscillator	Lead	Pad Type	Description
XTAL_IN	16	Analogue	For crystal or external clock input
XTAL_OUT	17	Analogue	Drive for crystal

UART	Lead	Pad Type	Description
UART_TX	28	CMOS output, tristate, with weak internal pull-up	UART data output
UART_RX	23	CMOS input with weak internal pull-down	UART data input
UART_RTS	24	CMOS output, tristate, with weak internal pull-up	UART request to send active low
UART_CTS	26	CMOS input with weak internal pull-down	UART clear to send active low

SPI	Lead	Pad Type	Description
SPI_CS#	41	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	43	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	39	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	42	CMOS output, tristate, with weak internal pull-down	Serial Peripheral Interface data output

PIO Port	Lead	Pad Type	Description
PIO[0]	2	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[1]	3	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	56	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	52	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line

PIO Port	Lead	Pad Type	Description
PIO[4]	35	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	36	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	37	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	33	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	53	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	54	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	51	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	1	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	21	Bidirectional	Programmable input/output line
AIO[1]	20	Bidirectional	Programmable input/output line
AIO[2]	19	Bidirectional	Programmable input/output line

Test and Debug	Lead	Pad Type	Description
RST#	38	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	40	CMOS input with strong internal pull-down	For test purposes only(leave unconnected)

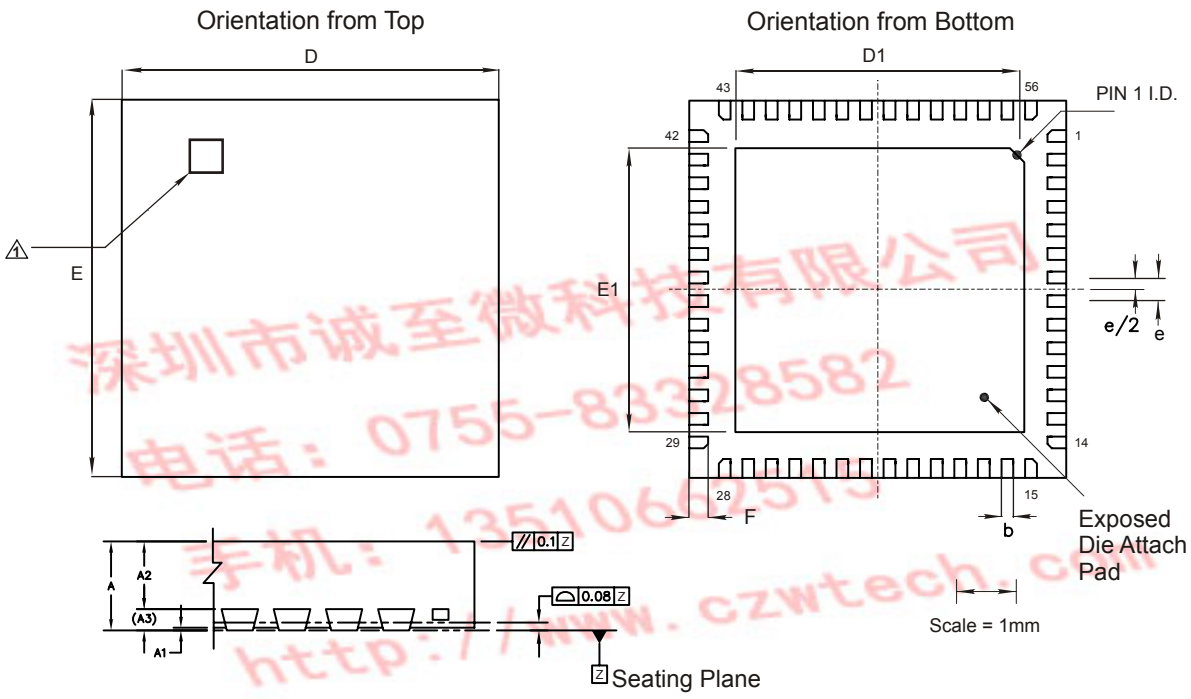
Codec	Lead	Pad Type	Description
MIC_P	14	Analogue	Microphone differential, Input P
MIC_N	15	Analogue	Microphone differential, Input N
SPKR_P	12	Analogue	Speaker differential output P or single ended output
SPKR_N	11	Analogue	Speaker differential output N

LED	Lead	Pad Type	Description
LED[0]	49	Open drain output	Current sink to drive LED
LED[1]	50	Open drain output	Current sink to drive LED

Power Supplies and Control	Lead	Pad Type	Description
VREGENABLE	4	CMOS input	Enable input terminal for both voltage regulators
VREG_IN	9	Regulator input	Linear regulator input
VREG_OUT	10	Regulator output	Linear regulator output
VDD_CHG	45	Charger input	Input for battery charger
BAT_P	46	Battery terminal +	Lithium Ion/Polymer battery positive terminal/Input connection for switch-mode regulator
BAT_N	48	Battery terminal -	Lithium Ion/Polymer battery negative terminal/Ground connection for switch-mode regulator
LX	47	Switch-mode regulator output	Switch-mode power regulator output
VDD_UART	22, 25	VDD	Positive supply for UART port. VDD_UART leads 22 and 25 must be connected together
VDD_PIO	55	VDD	Positive supply for PIO[3:0] and PIO[11:6]
VDD_PADS	44	VDD	Positive supply for all digital Input/ Output ports, SPI/PCM ports and PIO[7:4]
VDD_CORE	34	VDD	Positive supply for internal digital circuitry
VDD_RADIO	5	VDD/Regulator sense	Positive supply for RF circuitry
VDD_LO	8	VDD	Positive supply for local oscillator circuitry
VDD_ANA	13, 18	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VSS	-	VSS	Exposed Pad (downbond)

Unconnected Terminals	Lead	Description
NC	27, 29, 30, 31, 32	Leave unconnected

3.3 Package Dimensions



Description	56 Lead Quad Flat No-lead (QFN) Package			
Size	8 x 8 x 0.9mm			
Pitch	0.5mm			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.80	0.85	0.90	1 Pin 1 polarity mark
A1	0.00	0.035	0.05	
A2	-	0.65	0.67	
A3	-	0.203	-	
b	0.20	0.25	0.30	
D	-	8.00	-	
E	-	8.00	-	
e	-	0.5	-	
D1	5.95	6.05	6.15	
E1	5.95	6.05	6.15	
F	0.35	0.40	0.45	
JEDEC	MO-220			
Unit	mm			

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Figure 3.2: 56-lead QFN Package Dimensions

3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.9mm QFN 56-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern to be in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

3.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth Modem

4.1 RF Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

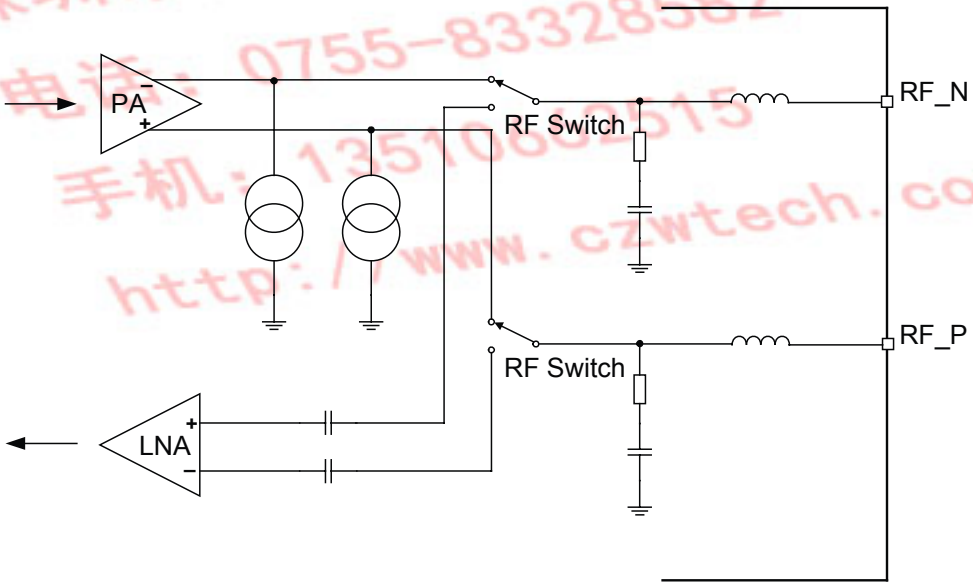

Figure 4.1: Simplified Circuit RF_N and RF_P

RF_N and RF_P require an external DC bias. The DC level must be set at VDD_RADIO.

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BC6110 to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BC6110 to be used in Class 2 and Class 3 radios without an external RF PA.

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

Including the basic rate modem allows BC6110 compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BC6110 supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3 bits. This is achieved using 2 new distinct modulation schemes. Table 4.1 and Figure 4.2 summarise these. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF ports, receiver, transmitter and synthesiser, with the baseband components described in Section 4.5.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.1: Data Rate Schemes

Figure 4.2: BDR and EDR Packet Structure

5 Clock Generation

BC6110 requires a Bluetooth reference clock frequency, it derives this from an externally connected crystal in the range 8MHz to 32MHz.

All BC6110 internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the external reference clock.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

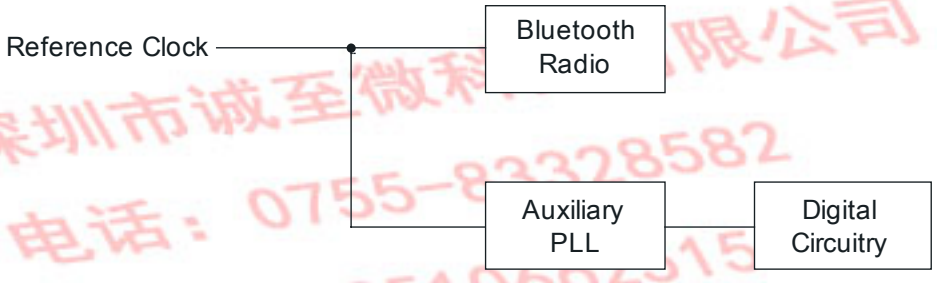

Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BC6110 is configured to operate with a chosen reference frequency. Configuration is by setting the PSKEY_ANA_FREQ for all frequencies with an integer multiple of 250kHz. The input frequency default setting for BC6110 is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

5.3 Crystal Oscillator: XTAL_IN and XTAL_OUT

BC6110 contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN, XTAL_OUT.

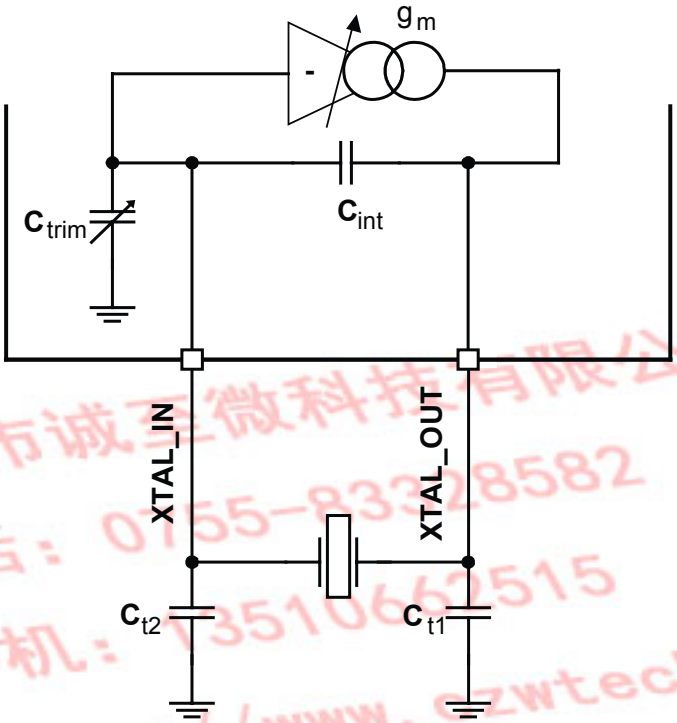

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Figure 5.2: Crystal Driver Circuit

Figure 5.3 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

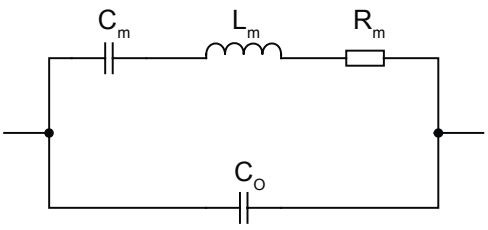

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Figure 5.3: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BC6110 contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	8	26	32	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 5.1: Crystal Specification

The BC6110 driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.3.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BC6110 provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated with Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.3.2 Frequency Trim

BC6110 enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 5.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = pullability \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(ppm/LSB)$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \cdot \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 5.3

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.3.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BC6110 uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\,\frac{(2\pi F_x)^2\,R_m\,((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\,(C_{t2} + C_{trim}))}{C_{t1}\,(C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BC6110 guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.3.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BC6110 crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it using Equation 5.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 5.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BC6110 driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.3.5 Crystal PS Key Settings

The BC6110 firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

BC6110 should be configured to operate with the chosen reference frequency.

6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 Programmable I/O (PIO) Parallel Ports

15 lines of programmable bidirectional I/O are provided.

Note:

> PIO[11:4] are powered from VDD_PADS and PIO[3:0] are powered from VDD_PIO. AIO[2:0] are powered from VDD_ANA.

Any of the PIO lines are configurable as button inputs or control outputs. Certain PIOs also have dedicated functions that are accessed using appropriate PS Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful in detecting when BC6110 is entering or leaving deep sleep.

Note:

> CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BC6110 has 3 general-purpose analogue interface pins, AIO[2:0], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 8-bit ADC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (output from AIO[0] only) and the XTAL and XTAL/2 clock frequency (output from AIO[0] and AIO[1]). When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

7 Memory Interface and Management

7.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is transferred between BC6110 and the air, or the host. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

7.3 Internal ROM

Internal ROM is provided for system firmware implementation.

8 Serial Interfaces

8.1 UART Interface

BC6110 has a standard UART serial interface that provides a simple communications channel for test and debug using RS232 protocol.

Figure 8.1: Universal Asynchronous Receiver

Figure 8.1 shows the 4 signals that implement the UART function. When BC6110 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, can implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using PS Keys.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 8.1: Possible UART Settings

The UART interface can reset BC6110 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 8.2 shows. If t_{BRK} is longer than the value, defined by PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature allows a host to initialise the system to a known state. Also, BC6110 can emit a break character that may be used to wake the host.

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Figure 8.2: Break Signal

Table 8.2 shows a list of commonly used baud rates and their associated values for the PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 8.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 8.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 8.2: Standard Baud Rates

8.1.1 UART Configuration While Reset is Active

The UART interface for BC6110 is tristate while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BC6110 reset is de-asserted and the firmware begins to run.

8.2 Programming and Debug Interface

Important Note:

The SPI is used to configure (using PS Keys) and debug the BC6110. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

BC6110 uses a 16-bit data and 16-bit address programming and debug interface. Transactions can occur when the internal processor is running or is stopped. For more information, see the *Using SPI Design Guide*.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

8.2.1 Instruction Cycle

The BC6110 is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 8.3: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BC6110 on the rising edge of the clock line SPI_CLK. When reading, BC6110 replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BC6110 offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.2.2 Multi-slave Operation

BC6110 should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BC6110 is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BC6110 outputs `0` if the processor is running or `1` if it is stopped.

8.3 I²C Interface

PIO[8:6] are used to form a master I²C interface. The interface is formed using software to drive these lines.

Note:

PIO lines need to be pulled-up through 4.7kΩ resistors.

The program memory for the BC6110 is internal ROM so the I²C interface can only connect to a serial EEPROM, Figure 8.3 shows an example. The EEPROM stores PS Keys and configuration information.

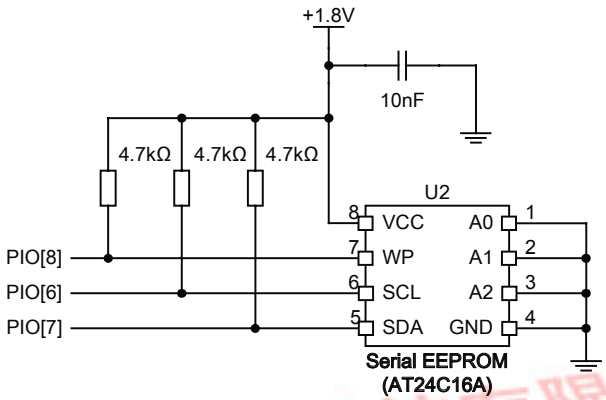

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Figure 8.3: Example EEPROM Connection

9 Audio Interface

The audio interface circuit consists of:

- Audio inputs and outputs
- Mono audio codec

9.1 Audio Input and Output

The audio input circuitry consists of an audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimisation of different microphones.

The audio output circuitry consists of a differential class A-B output stage.

9.2 Mono Audio Codec

The BC6110 audio codec is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8V power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The codec has an input stage containing a microphone amplifier, variable gain amplifier and a ΣΔ-ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The codec functional diagram is shown in below.

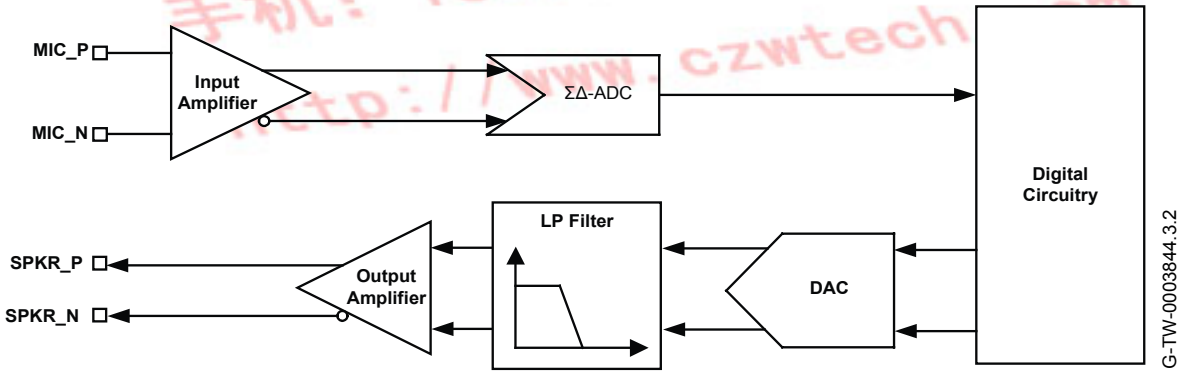

Figure 9.1: BC6110 Codec Diagram

9.2.1 Input Stage

A low noise variable gain amplifier amplifies the signal difference between inputs MIC_N and MIC_P. The input may be from either a microphone or line input. The amplified signal is then digitised by a second order - ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via a PS Key and has a 42dB range with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation with a microphone whereas the line input may be simply AC coupled. The following sections explain each of these modes. Single-ended signals are supported by BC6110: a single-ended signal may be driven into either MIC_N or MIC_P with the undriven input coupled to ground by a capacitor.

The signal to noise ratio is better than 60dB and distortion is less than -75dB.

9.2.2 Microphone Input

The BC6110 audio codec has been designed for use with microphones that have sensitivities between -60 and -40dBV. The sensitivity of -60dBV is equivalent to a microphone output of 1µA when presented with an input level of 94dB SPL and loaded with 1kΩ.Figure 9.2 shows how to bias the microphone.

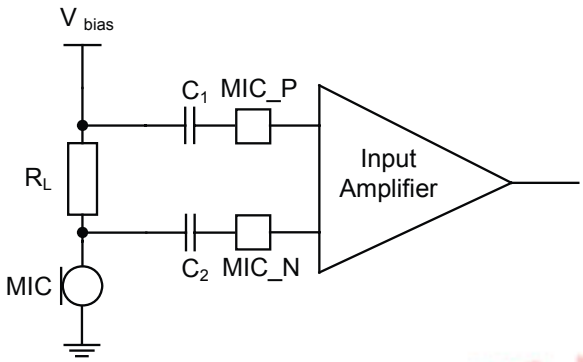

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Figure 9.2: BC6110 Microphone Biasing

The input impedance at MIC_N and MIC_P is typically 20kΩ. C1 and C2 should be 100nF. R_L sets the microphone load impedance and is normally between 1 and 2kΩ. Choose V_{bias} to suit the microphone and have sufficient low noise. It may be obtained by filtering the output of a PIO line.

9.2.3 Line Input

If the input gain is set to less than 21dB BC6110 automatically selects line input mode. In this mode the input impedance at MIC_N and MIC_P is increased to 130kΩ typical. At the minimum gain setting the maximum input signal level is 380mV rms. Figure 9.3 and Figure 9.4 show two circuits for line input operation and show connections for either differential or single-ended inputs.

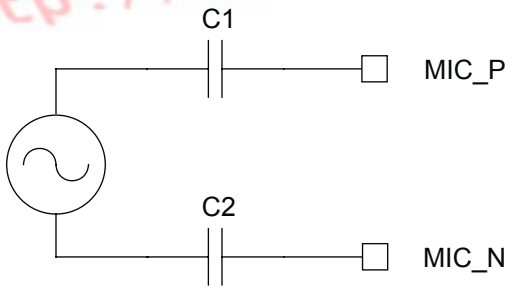

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Figure 9.3: Differential Microphone Input

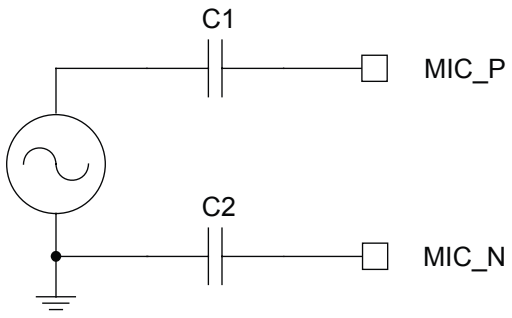

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Figure 9.4: Single-ended Microphone Input

Note:

C1 and C2 should be 15nF.

9.2.4 Output Stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR_P and SPKR_N. The output amplifier is capable of driving a speaker directly if its impedance is greater than 8Ω. The amplifier is stable with capacitive loads up to 500pF.

The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than -75dB.

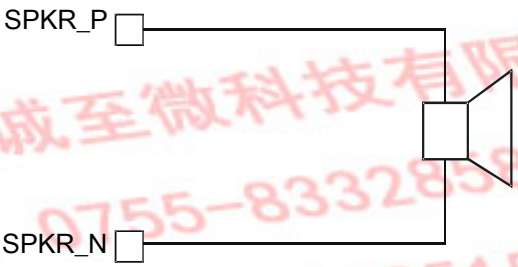

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Figure 9.5: Speaker Output

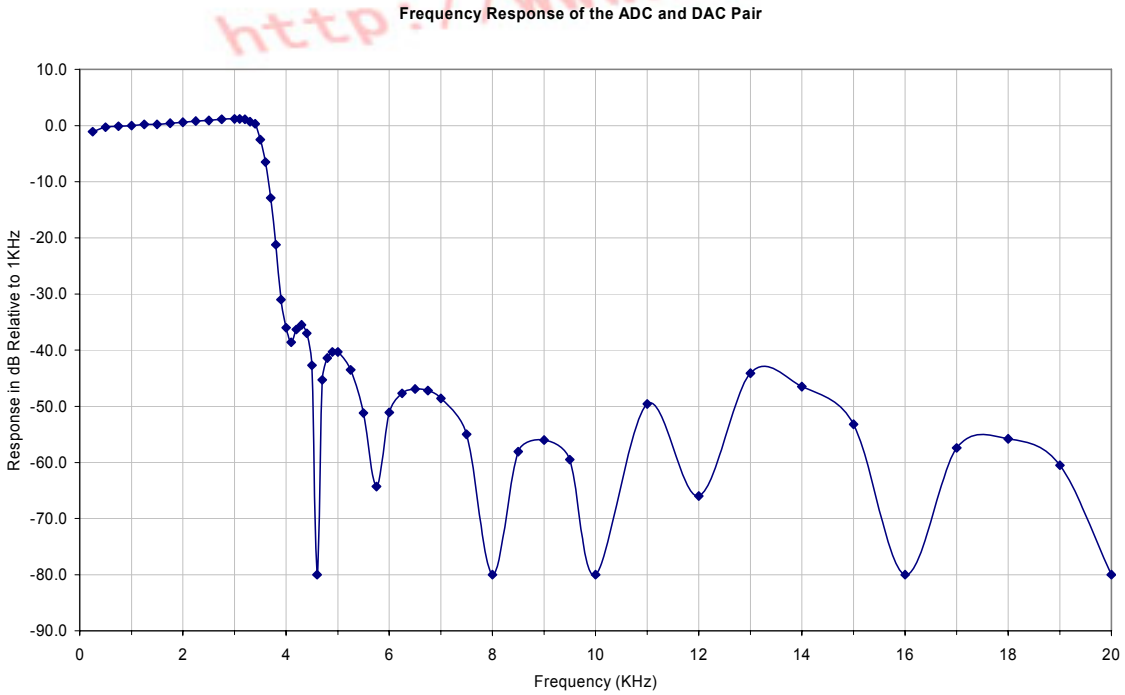


Figure 9.6: Frequency Response of the ADC and DAC Pair

9.2.5 Single-ended Speaker Termination

Certain applications require that a single-ended speaker termination scheme is used in place of the standard differential output. BC6110 allows the unused SPKR_N output to be disabled to reduce static power consumption, or alternatively, to be used to buffer the internal reference voltage that is used by the SPKR_P drive. It is also possible to externally decouple the voltage reference via an AIO.

9.2.6 Bass Cut (Wind Noise Reduction)

Digital enhancements have been made to the BC6110 mono codec to reduce wind noise. The wind noise filter rejects low frequencies present in the ADC signal. This is achieved by combining an analogue reconstruction filter and a digital filter located at the output of the ADC processing chain, see Figure 9.8.

The digital wind noise filter has been designed to compensate for the frequency response of a single-pole analogue high-pass filter with a 3dB cut-off frequency at 800Hz. The analogue high-pass filter characteristic is provided by the audio input resistance in conjunction with external AC coupling capacitors. Figure 9.7 shows a simulation of the frequency response for bass cut (wind noise reduction) digital enhancement.

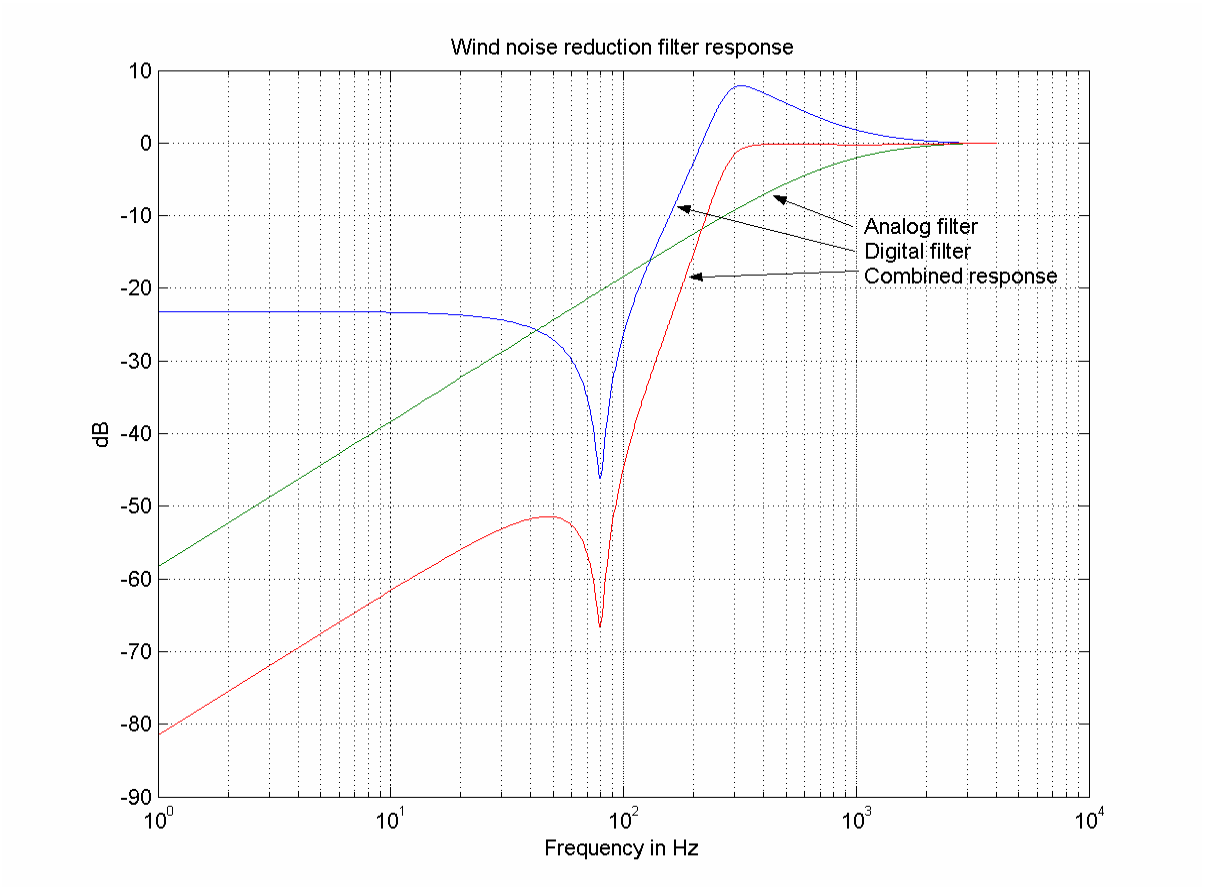


Figure 9.7: Simulated Wind Noise Reduction Filter Response

9.2.7 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BC6110 mono codec now incorporates the means to do this, see Figure 9.8.

9.2.8 Audio Codec Outline and Applicable Gains

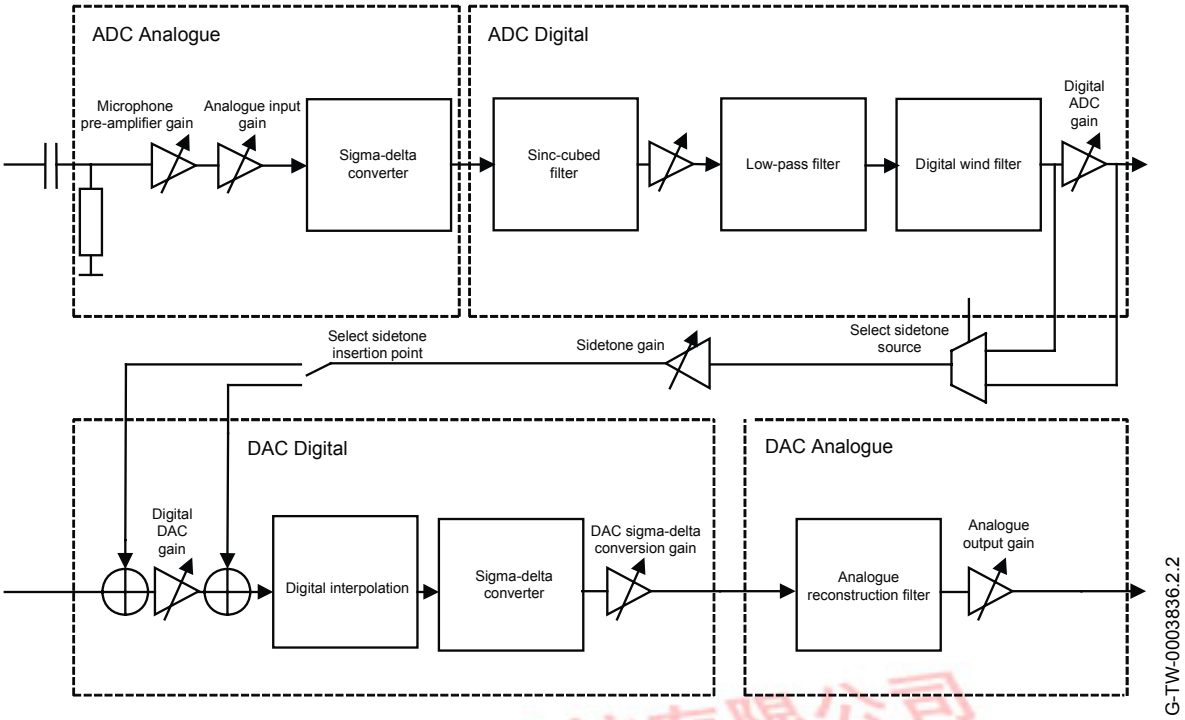


Figure 9.8: Audio Codec Outline and Applicable Gains

10 Power Supply

10.1 Power Regulators

BC6110 contains two 1.8V regulators, either of which can power the 1.8V supplies of the BC6110. The device pin VREGENABLE enables and disables both of these regulators.

10.2 Supply Domains and Sequencing

The 1.8V supplies are VDD_ANA, VDD_LO, VDD_RADIO and VDD_CORE. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other I/O supplies (VDD_PIO and VDD_PADS) is not important, however if the I/O supplies are powered before the 1.8V supplies all digital IO will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_LO, and VDD_RADIO should be connected directly to the 1.8V supply; a simple RC filter is recommended for VDD_CORE to reduce transients put back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

10.3 External Voltage Source

If supplying the 1.8V rails of BC6110 from an external voltage source, it is recommended that VDD_LO, VDD_RADIO, and VDD_ANA, should have less than 10mV rms noise levels between 0 to 10MHz. Also avoid single-tone frequencies.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption will jump to high levels.

10.4 Switch-mode Regulator

The on-chip switch-mode 1.8V regulator can be used to power the 1.8V supplies. The required external filter circuit should consist of a low resistance 33µH series inductor (between the LX terminal and the 1.8V supply), followed by a low ESR 4.7µF shunt capacitor (between the 1.8V supply and ground). For optimum efficiency the 33µH inductor must have low resistance. To optimise reliability and enable temperature derating, it must also be able to support at least 150mA.

It is recommended that the series resistance of tracks between the BAT_P and BAT_N terminals, the filter components and the external voltage source are minimised to maintain high efficiency power conversion and low supply ripple. The regulator may be enabled by the VREGENABLE pin, by the device firmware, or by the internal battery charger. The regulator is switched into a low power pulse skipping mode automatically when the device enters Deep-Sleep mode. When this regulator is not used the terminals BAT_P and LX must be grounded or left unconnected.

10.5 Linear Regulator

The on-chip 1.8V linear regulator may also be used to power the 1.8V dependent supplies. It is recommended that a smoothing circuit be used, consisting of an output regulator connected to ground via a 2.2Ω resistor and a series connected 2.2µF low ESR capacitor.

The regulator may be enabled by the VREGENABLE pin or by the device firmware. The regulator switches into a low power mode automatically when the device enters Deep-Sleep mode. When this regulator is not used the terminals VREG_IN and VREG_OUT must be grounded or left unconnected.

10.6 VREGENABLE Pin

The regulator enable pin, VREGENABLE enables and disables the BC6110 device if 1 of the on-chip regulators is used. The pin is active high and has a weak pull-down.

When the pin is pulled high the active regulator is enabled, allowing the device to boot-up. The firmware is then able to latch the regulator on and the VREGENABLE pin may be released.

10.7 Battery Charger

The battery charger is a constant current/constant voltage charger circuit and is suitable for Lithium Ion/Polymer batteries only. It must be used in conjunction with the switch-mode regulator as the two circuits share a connection with the battery terminal, BAT_P.

The constant current provided by the charger may be set between 25mA and 100mA typical, allowing different capacity batteries to be charged at their optimum rate. The required current setting is stored in ROM memory and read by the battery charger during the first boot-up sequence. The charger circuit also requires a float voltage calibration setting which must be measured for each device during production test. This should be stored in external PROM memory, and will be read by the battery charger during the boot-up sequence.

Whenever the charger is powered the switch-mode regulator is enabled automatically. Internal interfaces are provided to allow firmware to monitor the precise battery voltage and the status of the battery charger. The firmware may also disable the charger, for example, if termperature limits for safe charging are exceeded.

An LED connected to the terminal LED[0] will illuminate at full intensity when a battery is being charged.

When the charger supply is not connected to VDD_CHG the terminal must be left open.

Important Note:

Protection Module

Lithium Ion/Polymer batteries are capable of delivering high currents of several amperes when short-circuited. This can damage connecting wires and PCB components. More seriously, pressure can build up in the cell envelope, causing it to explode and injure the user.

CSR strongly suggests that Lithium Ion/Polymer batteries incorporate an integral protection module. This is typically a small IC and FET interposed between the battery body and its connecting wires. The protection module limits the short circuit current. Good modules will also prevent over-charge and over-discharge, which can also cause damage to the battery.

Additional Precautions

CSR also suggests that the following additional precautions are observed:

- The DC inlet socket used on the appliance should be of a proprietary design, preventing users from attaching the charger or supply connector for another appliance, e.g. a mobile phone or laptop computer. The use of popular 2.1mm and 2.5mm DC jack sockets must be avoided for this reason.
- Include a voltage limiting circuit (clamp) on the charger inlet. Remember that this circuit could be exposed to voltages as high as 30V (of either polarity) if a laptop computer power supply has been connected. Include a small fuse in series with the DC inlet, but prior to the clamp.
- Never bring the Lithium Ion/Polymer battery connections directly to charging pins on the outside of the appliance casing, where they could be short-circuited by keys in the user's pocket, for example.

Temperature Extremes

Some Lithium Ion/Polymer cells can be damaged by charging at temperature extremes (e.g., below 0°C or above 50°C). Consult the battery manufacturer for guidance.

For more information, see the CSR document *Lithium Ion/Polymer Battery Safety Information Note*.

10.8 LED Drivers

BC6110 includes two 4.2V tolerant pads dedicated to driving LED indicators. Both pads are controlled by firmware, while LED[0] can also be set by the battery charger.

The terminals are low output impedance open-drain outputs, so the LED must be connected in series with a current limiting resistor between the battery terminal or positive supply and the pad.

10.9 Reset, RST#

BC6110 is reset from several sources:

- RST# pin
- Power-on-reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RST# being active. It is recommended that RST# be applied for a period >5ms.

The power-on-reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tristate. The PIOs have weak pull-downs. Following a reset, BC6110 assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BC6110 is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BC6110 free runs, again at a safe frequency.

10.9.1 Pin States on Reset

Pin Name	State
PIO[11:0]	Input with weak pull-down
UART_TX	Output tristated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tristated with weak pull-up
UART_CTS	Input with weak pull-down
SPI_CS#	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tristated with weak pull-down
AIO[2:0]	Output tristated with weak pull-down
RST#	Input with weak pull-up
TEST_EN	Input with strong pull-down
RF_N	High impedance
RF_P	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 10.1: Pin States of BC6110 on Reset

10.9.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Data rate and RAM data remain available
- Cold Reset: Data rate and RAM data not available

11 Example Application Schematic

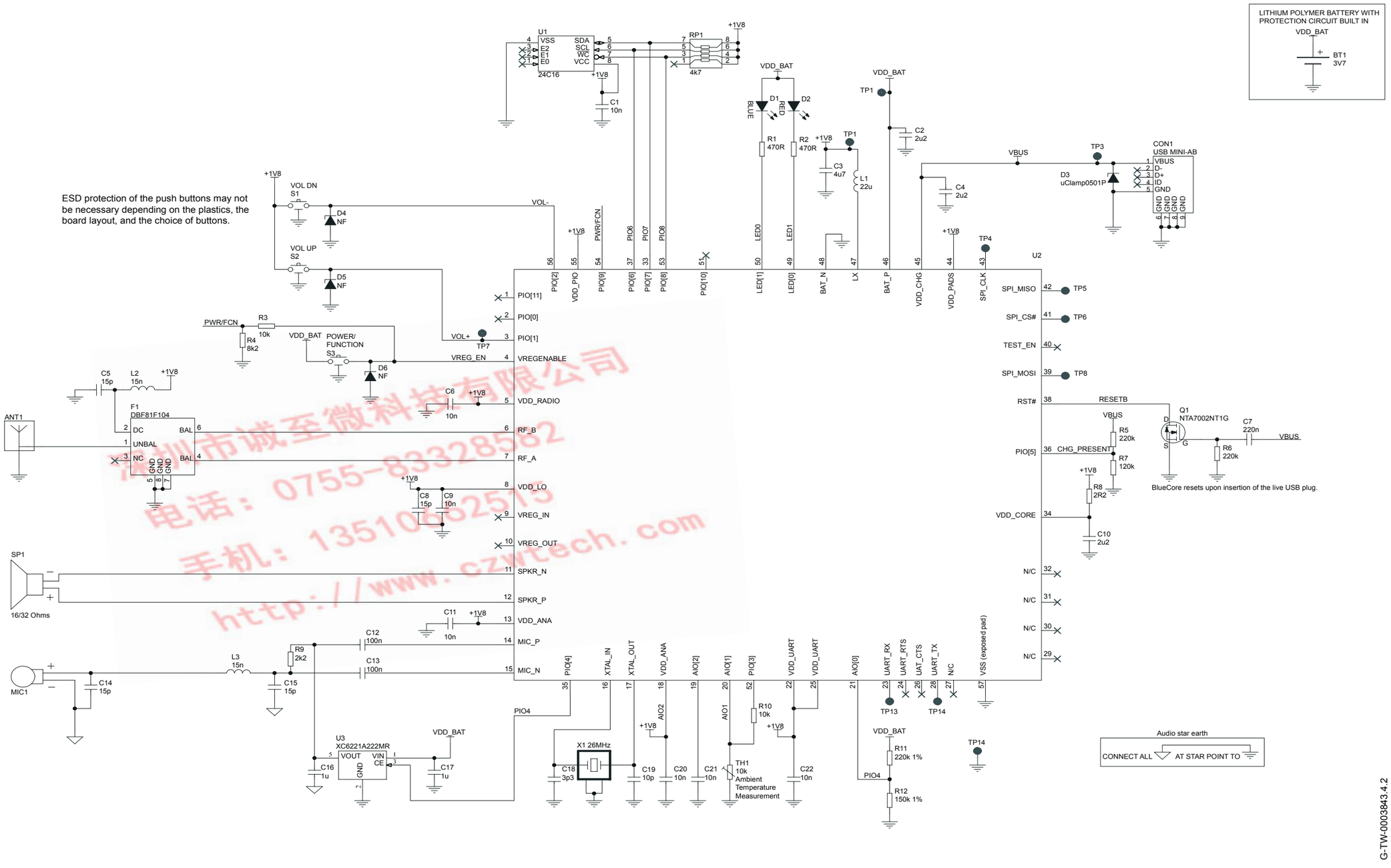


Figure 11.1: Example Application Schematic

12 Electrical Characteristics

12.1 ESD Precautions

BC6110 is classified as a JESD22-A114 class 2 product. Apply ESD static handling precautions during manufacturing.

12.2 Absolute Maximum Ratings

Rating	Min	Max
Storage temperature	-40°C	+150°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply voltage: VDD_PADS, VDD_PIO	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Supply Voltage: BAT_P, VREGENABLE and LED [1:0]	-0.4V	4.25V
Supply Voltage: VDD_CHG	-0.4V	6.5V
Other terminal voltages	VSS-0.4V	VDD+0.4V

12.3 Recommended Operating Conditions

Operating Condition	Min	Max
Operating temperature range	-20°C	70°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply voltage: VDD_PADS, VDD_PIO	1.7V	3.6V
Supply voltage: VREG_IN	2.2V	5.25V[(a)]
Supply voltage: BAT_P , VREGENABLE and LED [1:0]	2.5V	4.2V
Supply voltage: VDD_CHG	4.5V	6.5V

[(a)] The device will operate without damage with VREG_IN as high as 5.6V. However the RF performance is not guaranteed above 5.25V.

12.4 Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.2	-	5.25[a]	V
Output Voltage (I_{load} = 70mA)	1.70	1.78	1.9	V
Temperature Coefficient	-250	-	250	ppm/°C
Output Noise[b] [c]	-	-	1	mV rms
Load Regulation (I_{load} < 100mA)	-	-	50	mV/A
Settling Time[b] [d]	-	-	50	µs
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2	V
Quiescent Current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low-power Mode [e]				
Quiescent Current (excluding load, I_{load} < 100µA)	4	7	10	µA

[a] Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BC6110, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 5.25V.

[b] Regulator output connected to 47nF pure and 4.7µF 2.2 ESR capacitors.

[c] Frequency range is 100Hz to 100kHz.

[d] 1mA to 70mA pulsed load.

[e] Low-power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

12.5 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.5	-	4.2	V
Output voltage (I_{load} = 70mA)	1.70	1.78	1.9	V
Temperature coefficient	-250	-	250	ppm/°C
Normal Operation				
Output ripple	-	-	1	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	100	-	-	mA
Conversion effeciency (I_{load} = 70mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	-	60	-	mA
Low-power Mode [d]				
Output ripple	-	-	1	mV rms
Transient settling time [e]	-	-	700	µs
Maximum load current	20	-	-	mA
Minimum load current	0	-	-	µA
Conversion efficiency (I_{load} = 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz

[a] 1mA to 70mA pulsed load

[b] Locked to crystal frequency

[c] Current is limited on start-up to prevent excessive stored energy in the filter inductor. The regulator will operate with reduced efficiency until the current limiter is disabled during the firmware boot-up sequence

[d] Low-power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

[e] 100A to 1mA pulsed load

[f] Defines minimum period between pulses. Pulses are skipped at low current loads

12.6 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	-	6.5	V
Charging Mode (BAT_P rising to 4.2V)				
Supply current [a]	-	2	-	mA
Flat battery charge current[b]	-	4	-	mA

Battery Charger		Min	Typ	Max	Unit
Battery trickle charge current[c] [d] [e]	Maximum setting I-CTRL = 15	-	10	-	mA
	Minimum setting I-CTRL = 0	-	2.5	-	mA
Maximum battery fast charge current I-CTRL = 15[d]	Headroom[f] > 0.7V	-	100	-	mA
	Headroom[f] = 0.3V	-	50	-	mA
Minimum battery fast charge current I-CTRL = 0[d]	Headroom[f] > 0.7V	-	25	-	mA
	Headroom[f] = 0.3V	-	15	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set)[g]		4.17	4.2	4.23	V
Float voltage trim step size[g]		-	50	-	mV
Battery charge termination current[h]		-	10	-	%

[a] Current into VDD_CHG, does not include current delivered to battery (I (VDD_CHG) - I (BAT_P))

[b] BAT_P < 1.8V approx.

[c] 1.8V < BAT_P < Float voltage

[d] Charge current can be set in 16 equally spaced steps, under the control of a register setting I-CTRL

[e] Trickle charge threshold < BAT_P < Float voltage

[f] Headroom is defined as the difference between the VDD_CHG and BAT_P voltages

[g] Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

[h] Specified as a percentage of the Fast charge current

Standby Mode (BAT_P falling from 4.2V)	Min	Typ	Max	Unit
Supply current[a]	-	80	-	µA
Battery current	-	-40	-	µA
Battery recharge hysteresis[b]	100	-	200	mV

[a] Current into VDD_CHG, does not include current delivered to battery (I (VDD_CHG) - I (BAT_P))

[b] Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

Shutdown Mode (VDD_CHG too low)		Min	Typ	Max	Unit
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.9	-	V
	VDD_CHG falling	-	3.7	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V
Supply current		-	-	100	µA
Battery current		-1	-	0	µA

12.7 Digital Terminals

Input Voltage Levels		Min	Typ	Max	Unit
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.6V	-0.4	-	0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD + 0.4	V
Output Voltage Levels					
V_{OL} output logic level low I_o = 4.0mA	2.7V ≤ VDD ≤ 3.6V	-	-	0.2	V
	1.7V ≤ VDD ≤ 1.9V	-	-	0.4	V
V_{OH} output logic level high I_o = -4.0mA	2.7V ≤VDD ≤ 3.6V	VDD - 0.2	-	-	V
	1.7V ≤VDD ≤1.9V	VDD - 0.4	-	-	V
Input and Tristate Current					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		0.2	1.0	5.0	µA
I/O pad leakage current		-1	0	1	µA
C_I input capacitance		1.0	-	5.0	pF

12.8 Power on Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

12.9 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	8	26	32	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2	-	-	mS
Negative resistance[c]	870	1500	2400	Ω

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

12.10 Audio Codec, 15-bit Resolution

Analogue to Digital Converter	Min	Typ	Max	Unit
Input sample rate[a]	-	1	-	Msps
Output sample rate[b]	-	8	-	Ksps
Distortion and noise at 1kHz (relative to full scale)	-	-78	-75	dB

[a] Single bit, second order τ - Δ ADC clocked at 1MHz

[b] This is the decimated and filtered output at 15-bit resolution

Digital to Analogue Converter	Min	Typ	Max	Unit
Gain resolution	2.8	3	3.2	dB
Min gain[a]	-	-18	-	dB
Max gain[a]	-	3	-	dB

[a] 21dB gain range (under software control)

Microphone Amplifier	Min	Typ	Max	Unit
Input full scale at maximum gain	-	3	-	mV rms
Input full scale at minimum gain	-	350	-	mV rms
Gain resolution[a]	2.8	3	3.2	dB
Distortion at 1kHz	-	-	-78	dB
Input referenced rms noise[b]	-	5	-	µV rms
Bandwidth	-	20	-	kHz
Mic mode input impedance	-	20	-	kΩ
Input mode input impedance	-	130	-	Ω

[a] 42dB range of gain control (under software control)

[b] Noise in bandwidth from 100Hz to 4kHz gain setting >17dB

Loudspeaker Driver		Min	Typ	Max	Unit
Output voltage full-scale swing (differential)		-	2.0	-	V Pk-Pk
Output current drive (at full-scale swing)[a]		10	20	40	mA
Output full-scale current (at reduced swing)[b]		-	75	-	mA
Output -3dB bandwidth		-	18.5	-	kHz
Distortion and noise (relative to full scale) (32 load) differential		-	-75	-	dB
Allowed load	Resistive	8[c]	-	O.C.	Ω
Allowed load	Capacitive	-	-	500	pF

[a] Output for 0.1%THD, signal level of 2V Pk-Pk differential

[b] Output for 1%THD, signal level of 1V Pk-Pk differential

[c] Output swing reduced to 1.2V Pk-Pk differential with 1%THD or 0.1V Pk-Pk differential with 0.1%THD

13 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		HV3	30	10.21	mA
Slave	eSCO		EV3	30	11.91	mA
Slave	eSCO		2EV3	60	8.44	mA
Slave	eSCO		2EV3	30	12.55	mA
Slave	ACL	Sniff = 100ms	-	-	1.00	mA
Slave	ACL	Sniff = 500ms	-	-	0.46	mA
Slave	ACL	Sniff = 1280ms	-	-	0.35	mA
Master	SCO		HV3	30	10.38	mA
Master	eSCO		EV3	30	11.49	mA
Master	eSCO		2EV3	60	8.21	mA
Master	eSCO		2EV3	30	11.59	mA
Master	ACL	Sniff = 100ms	-	-	1.37	mA
Master	ACL	Sniff = 500ms	-	-	0.49	mA
Master	ACL	Sniff = 1280ms	-	-	0.38	mA

Note:

Current consumption values are taken with:

- BAT_P pin for switch-mode regulator = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected, with internal microphone bias circuit set to minimum current level
- Audio gateway transmits silence when SCO/eSCO channel is open
- LED's disconnected

14 CSR Green Semiconductor Products and RoHS Compliance

14.1 RoHS Statement

BC6110 where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

14.1.1 List of Restricted Materials

BC6110 is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

In addition, the following substances are not intentionally added to BC6110 devices:

- Halogenated flame retardant
- Antimony (Sb) and Compounds, including Antimony Trioxide flame retardant
- Polybrominated Diphenyl and Biphenyl Oxides
- Tetrabromobisphenol-A bis (2,3-dibromopropylether)
- Asbestos or Asbestos compounds
- Azo compounds
- Organic tin compounds
- Mirex
- Polychlorinated napthelenes
- Polychlorinated terphenyls
- Polychlorinated biphenyls
- Polychlorinated/Short chain chlorinated paraffins
- Polyvinyl Chloride (PVC) and PVC blends
- Formaldehyde
- Arsenic and compounds (except as a semiconductor dopant)
- Beryllium and its compounds
- Ethylene Glycol Monomethyl Ether or its acetate
- Ethylene Glycol Monoethyl Ether or its acetate
- Halogenated dioxins and furans
- Persistent Organic Pollutants (POP), including Perfluorooctane sulphonates
- Red phosphorous
- Ozone Depleting Chemicals (Class I and II): Chlorofluorocarbons (CFC) and Halons
- Radioactive substances

For further information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products.*

15 CSR Bluetooth Software Stack

BC6110 is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU.

The BC6110 software architecture allows Bluetooth processing and the application program to be run on the internal RISC MCU. The upper layers of the Bluetooth stack, above the HCI, are run on-chip.

15.1 BC6110 Low-cost Mono Headset Solution Development Kit

CSR's BC6110 low-cost mono headset solution development kit for BC6110, order code DK-BC-6110-1A, includes a headset demonstrator board, music and voice dongle and necessary interface adapters and cables. In conjunction with the BlueVox Configurator tool and other supporting utilities the development kit provides the best environment for designing a mono headset solution with BC6110.

15.2 BC6110 Low-cost Mono Headset Solution Software (BC6110A14)

- The CSR mono headset ROM software supports HFP1.5 and HSP1.1. Advanced features in these specifications are supported, including three-way calling.
- Bluetooth v2.1 + EDR specification is supported in the ROM software including Secure Simple Pairing.
- Proximity Pairing (headset initiated pairing) for greatly simplifying the out-of-box pairing process, for more information see Section 15.3.
- Most of the CSR mono headset ROM software features can be configured on the BC6110 using the BlueVox Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions. The tool can be used to read and write headset configurations directly to the EEPROM or alternatively to a PSR file. Configurable headset features include:
  - Bluetooth v2.1 + EDR specification features
  - Reconnection policies, e.g. reconnect on power on
  - Audio features, including default volumes
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for Last Number redial
  - LED indications for states, e.g. headset connected, and events, e.g. power on
  - Indication tones for events and ringtones
  - HFP1.5 supported features
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
- The BC6110 low-cost mono headset solution has undergone extensive interoperability testing to ensure that it will work with the majority of phones on the market

15.3 Proximity Pairing

Proximity Pairing is headset intiated pairing and it simplifies the out-of-box pairing process. Proximity Pairing allows the headset to find the closest discoverable phone. The headset then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus in order to pair with the new headset.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the headset pairing is with a PIN code
- For a Bluetooth v2.1 phone the headset pairing is without a PIN code

15.3.1 RSSI Pair

Proximity pairing is based on finding and pairing with the closest phone. In order to do this, the headset finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and is defined as the closest phone or the RSSI pair.

For Proximity Pairing to work well:

- Put the headset and phone close to each other (touching if possible)
- Power on the headset, the headset realises that there are no previously paired devices and enters RSSI pairing mode
- In RSSI pairing mode, the headset attempts to pair with the closest phone it can find. The headset is also discoverable so that if a phone attempts to discover the headset, then the headset can be discovered in the conventional way

- The RSSI pairing process requires the phone to be in discoverable mode
- Use a Bluetooth v2.1 phone so no PIN code entry is required
- Do not use a phone with limited discoverability

15.3.2 Proximity Pairing Configuration

Proximity Pairing is configurable using the BlueVox Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions.

16 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART	QFN 56-lead (Pb free)	8 x 8 x 0.9mm, 0.5mm pitch	Tape and reel	BC6110A14-IQQA-R

Note:

BC6110 is a ROM-based device where the product code has the form BC6110Axx. Axx is the specific ROM-variant, A14 is the ROM-variant for BC6110 Low-cost Mono Headset Solution.

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

17 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

17.1 Tape Orientation

Figure 17.1 shows the BC6110 packing tape orientation.

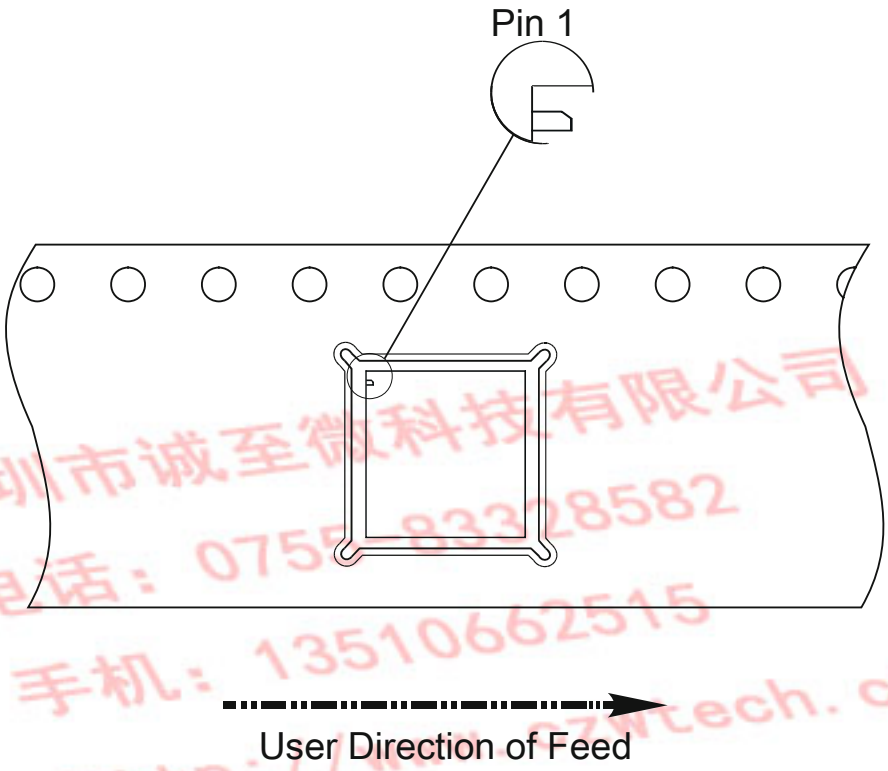
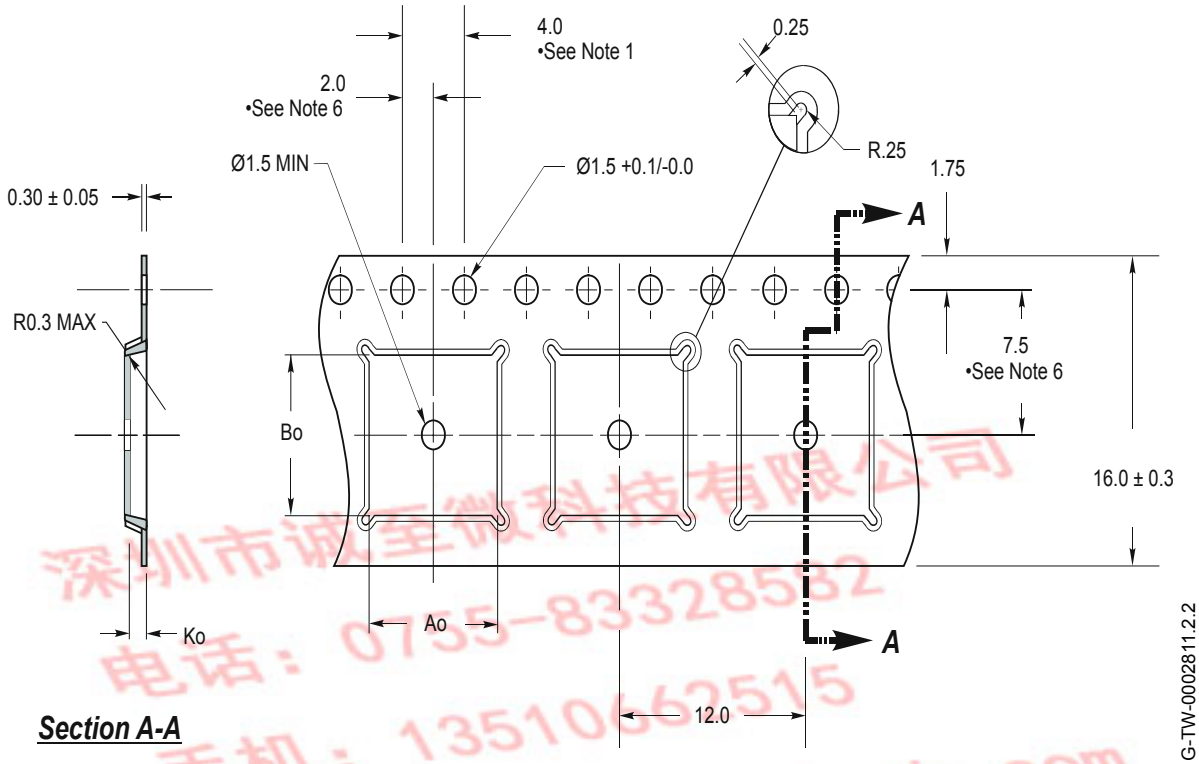


Figure 17.1: BC6110 Tape Orientation

G-TW-0002812.2.2

17.2 Tape Dimensions



Section A-A

A_0	B_0	K_0	Unit	Notes
8.3	8.3	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±TBD 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

17.3 Reel Information

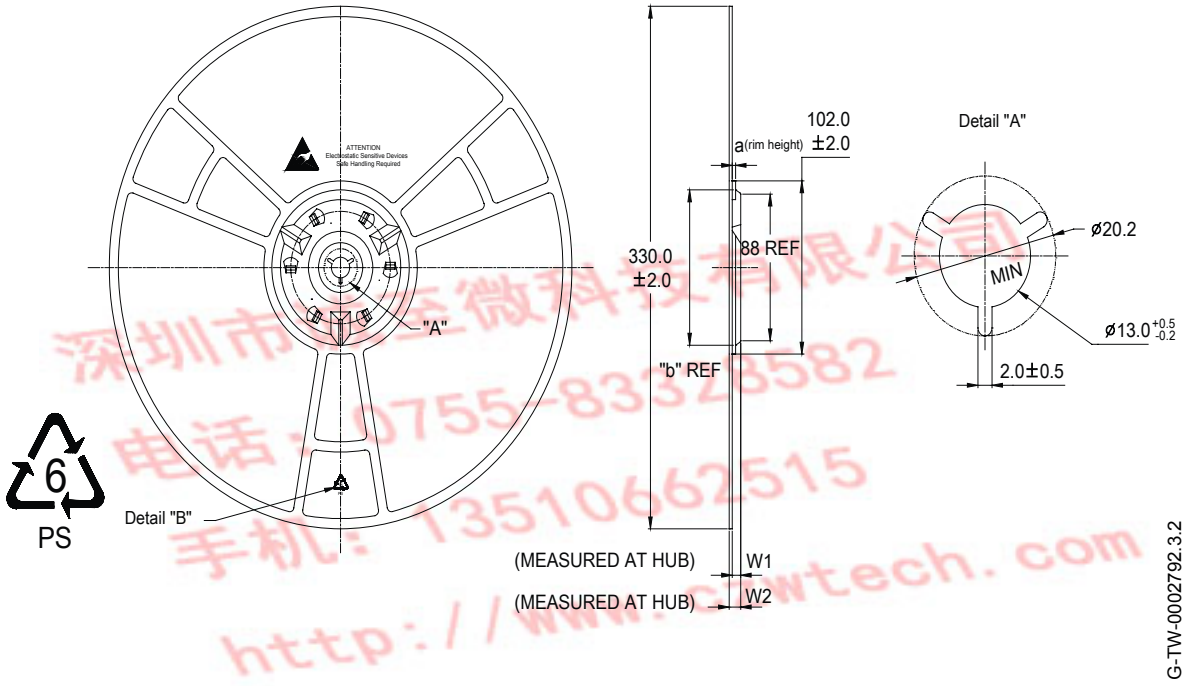


Figure 17.2: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.9mm QFN	16	4.5	98.0	16.4 (0.3/-0.2)	19.1	mm

17.4 Moisture Sensitivity Level

BC6110 is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

18 Document References

Document	Reference
Core Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
IC Packing and Labelling Specification	CS-112584-SPP
Lithium Ion/Polymer Battery Safety Information Note	bcore-an-057P
Selection of I²C EEPROMS for Use with BlueCore	bcore-an-008Pb
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 27 December 2006
Using SPI Design Guide	CS-126179-UGP

Terms and Definitions

Term	Definition
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
BIST	Built-In Self-Test
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CFC	Chlorofluorocarbon
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended SCO
ESD	Electrostatic Discharge
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HFP	Hands-Free Profile
HSP	HeadSet Profile
I^2C	Inter-Integrated Circuit Interface
I/O	Input/Output
IF	Intermediate Frequency
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
LC	An inductor (L) and capacitor (C) network
LNA	Low Noise Amplifier
MCU	MicroController Unit
MISO	Master In Slave Out
MMU	Memory Management Unit
NSMD	Non Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PIN	Personal Identification Number

Term	Definition
PIO	Programmable Input/Output
POP	Persistent Organic Pollutants
ppm	parts per million
PS Key	Persistent Store Key
PVC	Poly Vinyl Chloride
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SPI	Serial Peripheral Interface
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access