Features

- Fully Qualified Bluetooth v2.1 + EDR system
- Piconet and Scatternet Support
- Minimum External Components
- Low-Power 1.5V Operation, 1.8V to 3.6V I/O
- Integrated 1.8V and 1.5V Regulators
- UART to 4Mbaud
- SDIO (Bluetooth Type A)/CSPI Interface
- Deep Sleep SDIO Operation
- 3.21 x 3.49 x 0.6mm (max.), 0.4mm pitch WLCSP
- Support for 802.11 Coexistence
- RoHS Compliant

BlueCore™6-ROM (WLCSP)

Single Chip Bluetooth® v2.1 + EDR System

Advance Information Data Sheet for BC63B239A

September 2007

General Description

The **BlueCore™6-ROM (WLCSP)** is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including *enhanced data rates* (EDR) to 3Mbits/s.

With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.1 + EDR of the specification for data and voice communications.

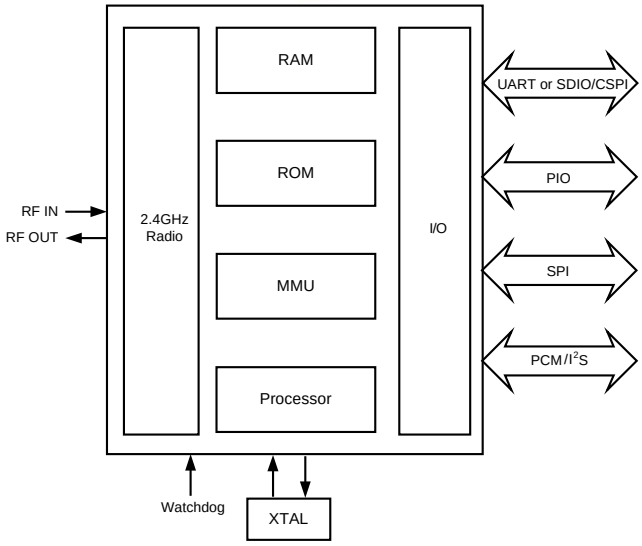

Figure 1: System Architecture

Applications

- Cellular handsets
- *Personal Digital Assistants* (PDAs)
- Automotive
- Personal Navigation Devices

BlueCore6-ROM (WLCSP) has been designed to reduce the number of external components required which ensures production costs are minimised.

BlueCore6-ROM (WLCSP) includes AuriStream, which offers significant power reduction over the CVSD based system when used at both ends of the link.

The device incorporates auto-calibration and *built-in self-test* (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification.

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of coexistence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

BlueCore™6-ROM (WLCSP) Product Data Sheet

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BlueCore™6-ROM (WLCSP) Product Data Sheet

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1 Status Information

The status of this Data Sheet is Advance Information.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore6-ROM (WLCSP) devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

2 Device Details

Bluetooth Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- No external trimming is required in production
- Bluetooth v2.1 + EDR Specification compliant

Bluetooth Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB

Bluetooth Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 16 and 26MHz or an external clock between 12 and 52MHz

Baseband and Software

- AuriStream (16, 24, 32, 40 kbps) CODEC
- Internal 48kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.1 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- SDIO and CSPI
- Synchronous serial interface up to 4Mbits/s for system debugging
- UART interface with programmable data rate up to 4Mbaud
- Bi-directional serial programmable audio interface supporting PCM and I^2S formats

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Clock request output to control an external clock
- Device can run in low power modes from an external 32768Hz clock signal
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Auto Baud Rate setting, subject to host interface in use
- On-chip linear regulators: 1.8V output from typical 2.7-5.5V input to power I/O ring (load current 100mA) and second low dropout linear regulator producing 1.5V core voltage from 1.8V
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in the configuration:

- Standard HCI over UART

Package Options

- 51 ball 3.21 x 3.49 x 0.6mm (max.), 0.4mm pitch regular grid WLCSP

3 Device Diagram

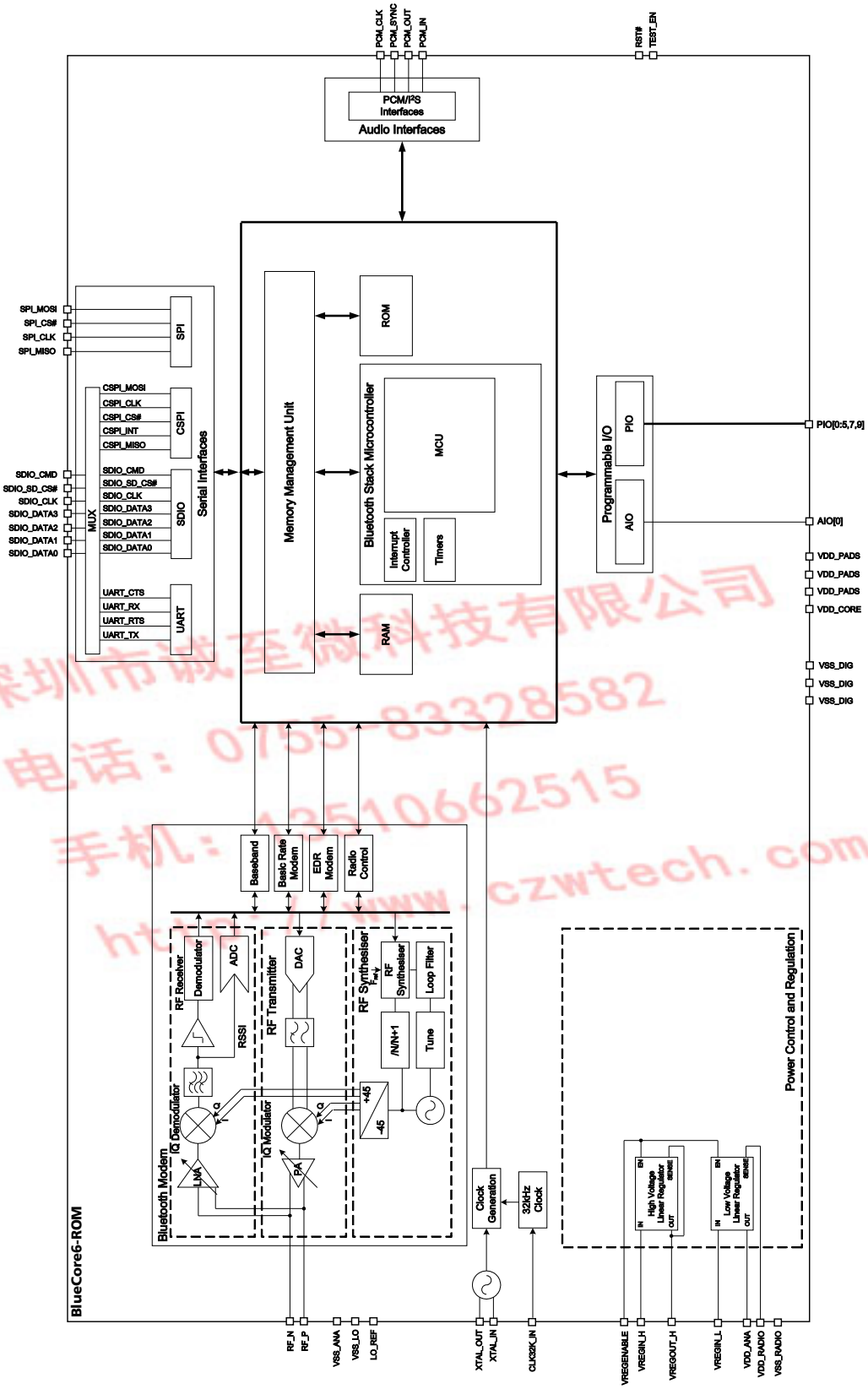


Figure 3.1: Device Diagram

4 Package Information

4.1 Package Information

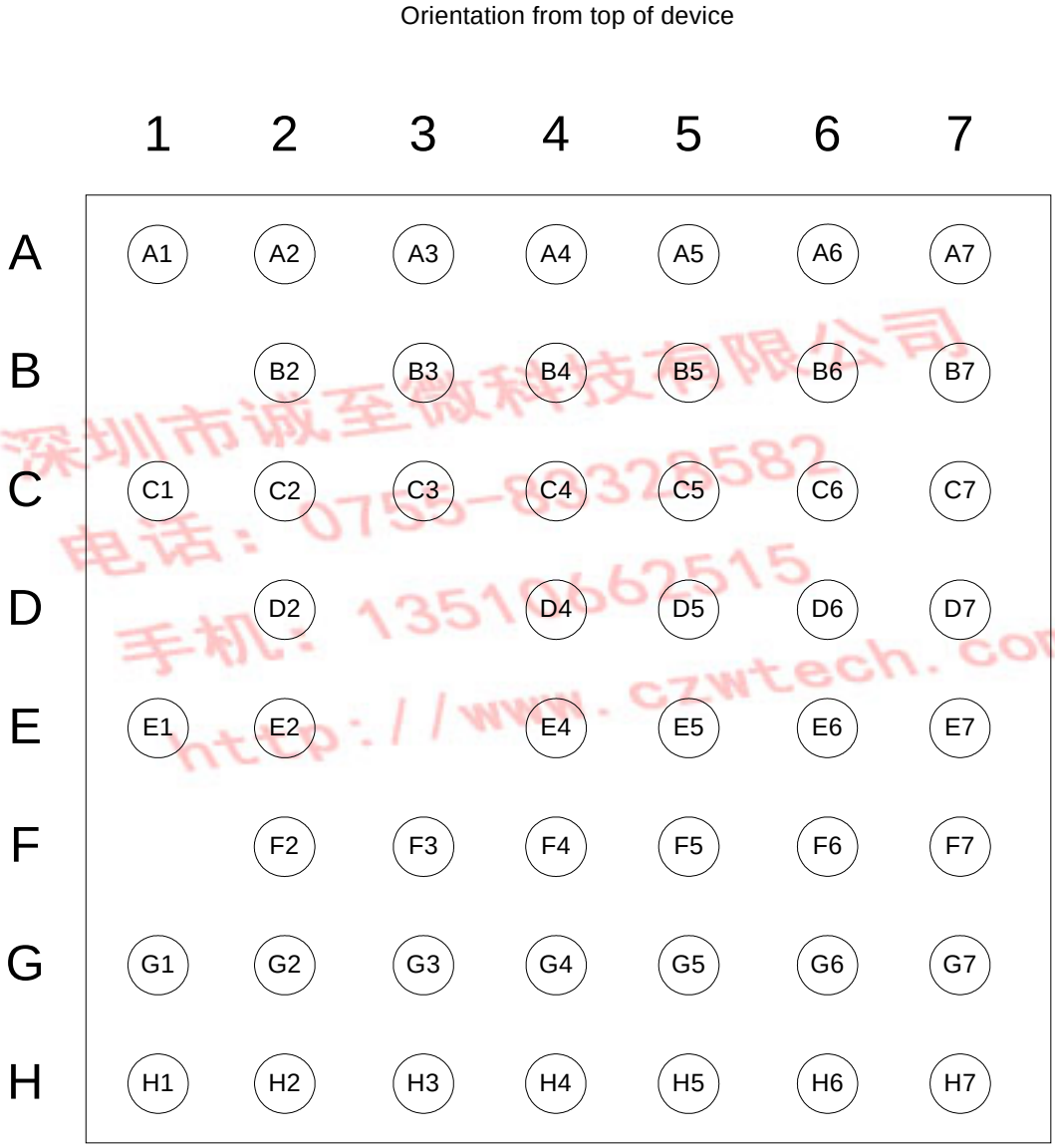


Figure 4.1: BlueCore6-ROM (WLCSP) Device Pinout

4.2 Device Terminal Functions

Bluetooth Radio	Ball	Pad Type	Supply Domain	Description
RF_N	E1	RF	RADIO	Transmitter output/switched receiver input
RF_P	F2	RF	RADIO	Complement of RF_N

Synthesiser and Oscillator	Ball	Pad Type	Supply Domain	Description
XTAL_IN	A3	Analogue	ANA	For crystal or external clock input
XTAL_OUT	A2	Analogue	ANA	Drive for crystal
LO_REF	B3	Analogue	ANA	Reference voltage decoupling
CLK_32K	E6	Input with weak internal pull-down	PADS	Dedicated 32kHz external reference clock input

SPI Interface	Ball	Pad Type	Supply Domain	Description
SPI_MOSI	G2	Input, with weak internal pull-down	PADS	SPI data input
SPI_CS#	F4	Bi-directional with weak internal pull-down	PADS	Chip select for Serial Peripheral Interface (SPI), active low
SPI_CLK	G3	Bi-directional with weak internal pull-down	PADS	SPI clock
SPI_MISO	H1	Output, tri-state, with weak internal pull-down	PADS	SPI data output

SDIO/CSPI/UART Interfaces[a]	Ball	Pad Type	Supply Domain	Description
SDIO_DATA[0]	G7	Output, tri-state, with weak internal pull-down	PADS	Synchronous data input/output
CSPI_MISO				CSPI data output
UART_TX				UART data output, active high
SDIO_DATA[1]	F6	Input, with weak internal pull-down	PADS	Synchronous data input/output
CSPI_INT				CSPI data input
UART_RTS				UART request to send, active low
SDIO_DATA[2]	F7	Bi-directional with weak internal pull-down	PADS	Synchronous data input/output
UART_RX				UART data input, active high
SDIO_DATA[3]	G6	Bi-directional with weak internal pull-down	PADS	Synchronous data input/output
CSPI_CS#				Chip select for CSR Serial Peripheral Interface (CSPI), active low
UART_CTS				UART clear to send, active low
SDIO_CLK	H7	Bi-directional with weak internal pull-down	PADS	SDIO Clock
CSPI_CLK				CSPI Clock
SDIO_CMD	D6	Input, with weak internal pull-down	PADS	SDIO data input
CSPI_MOSI				CSPI data input
SDIO_SD_CS#	E5	Input with weak internal pull-down	PADS	SDIO chip select to allow SDIO Accesses

[a] See Section 9 for more information.

PCM Interface[a]	Ball	Pad Type	Supply Domain	Description
PCM_OUT	G5	Output, tri-state, with weak internal pull-down	PADS	Synchronous data output
PCM_IN	F5	Input, with weak internal pull-down	PADS	Synchronous data input
PCM_SYNC	G4	Bi-directional with weak internal pull-down	PADS	Synchronous data sync
PCM_CLK	H2	Bi-directional with weak internal pull-down	PADS	Synchronous data clock

[a] The Digital Audio Interface (I^2S) shares the same pins as the PCM interface. For more information about I^2S, see section 10.2

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[9]	C7	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[7]	D5	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[5]	B7	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[4]	E7	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[3]	C6	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[2]	C5	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[1]	B5	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
PIO[0]	C4	Bi-directional with programmable strength internal pull-up/down	PADS	Programmable input/output line
AIO[0]	B4	Bi-directional	ANA	Programmable input/output line

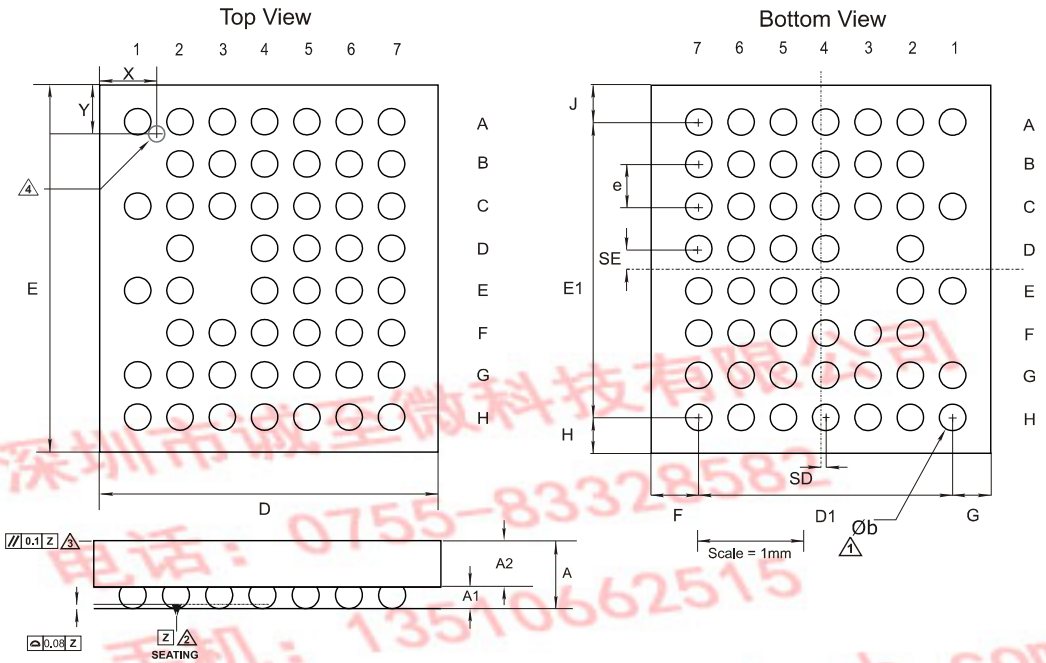
Test and Debug	Ball	Pad Type	Supply Domain	Description
RST#	E4	Input with weak internal pull-up	PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	D4	Input with strong internal pull-down	PADS	For test purposes only (leave unconnected)

Power Supplies Control	Ball	Description
VREGENABLE	A6	Take high to enable low and high voltage regulators

Power Supplies	Ball	Description
VREGIN_L	B2	Input to internal low-voltage regulator
VREGIN_H	A5	Input to internal high-voltage regulator
VREGOUT_H	A4	High-voltage regulator output
VDD_PADS	A7, H3,H6	Positive supply for digital input/output ports including PIO [0:5, 7, 9]
VDD_CORE	D7	Positive supply for internal digital circuitry
VDD_RADIO	F3	Positive supply for RF circuitry
VDD_ANA	A1	Positive supply for analogue circuitry, AIO[0]. Output from internal 1.5V regulator
VSS_ANA	C3	Ground connections for analogue circuitry
VSS_RADIO	G1	Ground connections for RF circuitry
VSS_LO	C1	Ground connections for VCO and synthesiser
VSS_DIG	B6, H4, H5	Ground connections for digital I/O circuitry

Unconnected Terminals	Ball	Description
N/Cs	C2, D2, E2	Leave unconnected

4.3 Package Dimensions



Description	51-Ball Wafer-Level Chip Scale Package (WLCSP)			
Size	3.21 x 3.49 x 0.6mm (max.)			
Pitch	0.4mm			
Package Ball Land	240µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			0.60	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1		0.2		
A2		0.37		
b		0.25		(2) Datum Z is defined by the spherical crowns of the solder balls
D	3.01	3.11	3.21	
E	3.29	3.39	3.49	
e		0.4		(3) Parallelism measurement shall exclude any effect of mark on top surface of package
D1		2.4		
E1		2.8		(4) Topside-polarity mark. The dimensions of the polarity mark are 0.3mm diameter.
F	0.300	0.450	0.500	
G	0.310	0.360	0.410	
H	0.294	0.344	0.394	
J	0.299	0.349	0.399	
SD		0.044		
SE		0.200		
X		TBD		
Y		TBD		
JEDEC	Non JEDEC			
Unit	mm			

Figure 4.2: BlueCore6-ROM (WLCSP) Package Dimensions

4.4 PCB Design and Assembly Considerations

4.4.1 51 Ball 3.21 x 3.49 x 0.6mm (max.), 0.4mm pitch WLCSP Package

The following list details the recommendations to achieve maximum board-level reliability of the 3.21 x 3.49 x 0.6mm (max.), 0.4mm pitch WLCSP Package.

- *Non-solder mask defined* (NSMD) lands (lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be employed to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred. This trace should be as thin as possible, taking into consideration its current carrying and the *radio frequency* (RF) requirements.
- CSR recommends 35 micron thick (1oz.) copper lands rather than 17 micron thick (1/2 oz.), because this results in a greater standoff, which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be 240µm +/-10µm to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process, because this adds to the final volume of solder in the joint, therefore increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5 micron to prevent brittle gold/tin intermetallics forming in the solder.

5 Bluetooth RF Interface Description

5.1 Bluetooth Radio Ports

5.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair. On transmit their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The package parasitics can be represented as an equivalent series inductance.

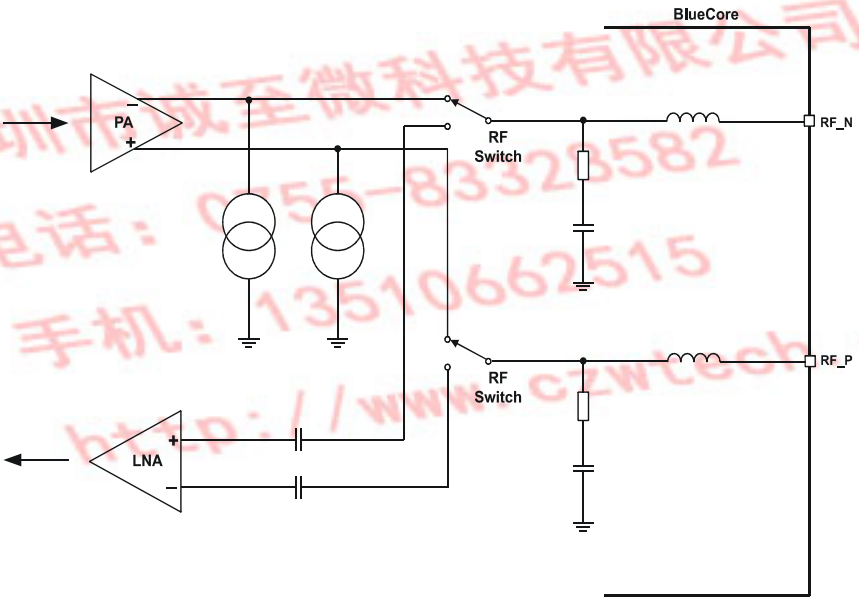


Figure 5.1: Simplified Circuit RF_N and RF_P

The DC level must be set at VDD_RADIO.

5.2 Bluetooth Receiver

The receiver features a near-zero *Intermediate Frequency* (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the *Low Noise Amplifier* (LNA) input allows the receiver to be used in close proximity to *Global System for Mobile Communications* (GSM) and *Wideband Code Division Multiple Access* (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital *Frequency Shift Keying* (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore6-ROM (WLCSP) to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the Demodulator contains an ADC which is used to digitise the IF received signal. This information is then passed to the EDR modem. See Figure 3.1

5.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

5.2.2 RSSI Analogue to Digital Converter

An *Analogue to Digital Converter* (ADC) is used to implement fast *Automatic Gain Control* (AGC). The ADC samples the *Received Signal Strength Indicator* (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

5.3 Bluetooth Transmitter

5.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

5.3.2 Power Amplifier

The internal *Power Amplifier* (PA) has a maximum output power of +6dBm. This allows BlueCore6-ROM (WLCSP) to be used in Class 2 and Class 3 Bluetooth radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

5.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external *Voltage Controlled Oscillator* (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

6 Clock Generation

6.1 Clock Input and Generation

BlueCore6-ROM (WLCSP) requires a Bluetooth reference crystal clock frequency of between 12MHz and 52MHz from either an externally connected crystal, or from an external TCXO source.

All BlueCore6-ROM (WLCSP) internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 12MHz to 52MHz reference clock source, or an external reference clock frequency of 32.768kHz, or an internally generated reference clock frequency of 1kHz.

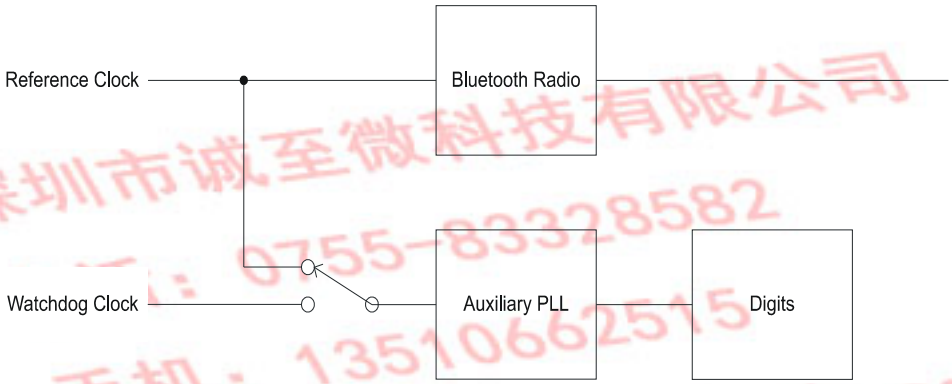


Figure 6.1: Clock Architecture

The auxiliary PLL may use either clock source. The clock to the digital logic is the same in both cases. The use of the watchdog clock is determined with respect to Bluetooth operation in low power modes.

6.1.1 Input Frequencies and PS Key Settings

BlueCore6-ROM (WLCSP) should be configured to operate with the chosen reference frequency. This is accomplished by setting `PSKEY_ANA_FREQ` (`0x01FE`) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore6-ROM (WLCSP) is 26MHz depending on the software build. For full details, see the software release note for the specific build at www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz. Hence 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1FE) (Units of 1kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 6.1: PS Key Values for CDMA/3G Phone TCXO

6.2 External Reference Clock

A 32kHz clock can be applied to either AIO[0] or CLK32K_IN.

If the external clock is applied to the analogue pad AIO[0], the digital signal should be driven with a maximum 1.5V. The CLK32K_IN pad is in the VDD_PADS domain with all the other digital I/O pads and is driven in the range 1.7V to 3.6V.

6.2.1 Clock Start Up Delay

BlueCore6-ROM (WLCSP) hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore6-ROM (WLCSP) firmware provides a software function that extends the system clock request signal by a period stored in `PSKEY_CLOCK_STARTUP_DELAY`. This value is set in milliseconds from 1-31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore6-ROM (WLCSP) as low as possible. BlueCore6-ROM (WLCSP) consumes about 2mA of current for the duration of `PSKEY_CLOCK_STARTUP_DELAY` before activating the firmware.

6.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

BlueCore6-ROM (WLCSP) contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN and XTAL_OUT.

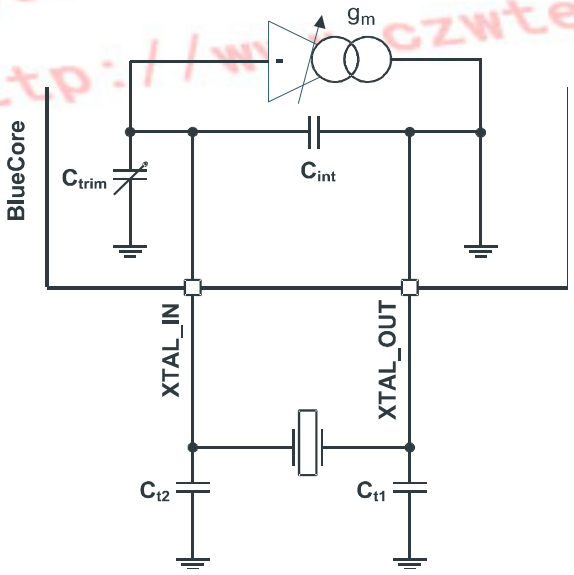


Figure 6.2: Crystal Driver Circuit

Figure 6.3 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

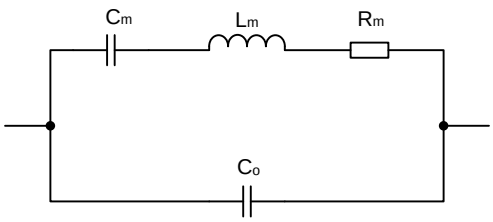


Figure 6.3: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore6-ROM (WLCSP) contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	16MHz	26MHz	26MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-
Transconductance	2.0mS	-	-

Table 6.2: Crystal Specification

The BlueCore6-ROM (WLCSP) driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

6.3.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore6-ROM (WLCSP) provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence, slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated with Equation 6.1.

$$C_l = C_{\text{int}} + \frac{(C_{t2} + C_{trim})C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 6.1: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

6.3.2 Frequency Trim

BlueCore6-ROM (WLCSP) enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the `PSKEY_ANA_FTRIM` (`0x1f6`). Its value is calculated as follows:

$$C_{trim} = 110\text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

Equation 6.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 110fF for each least significant bit increment of `PSKEY_ANA_FTRIM`.

The frequency trim is described by Equation 6.3.

$$\frac{\Delta(F_X)}{F_X} = \text{pullability} \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right) (\text{ppm/LSB})$$

Equation 6.3: Frequency Trim

Where Fx is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 0 to 63.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 6.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_0)^2}$$

Equation 6.4: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 6.3.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

6.3.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore6-ROM (WLCSP) uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 6.5.

$$g_m > 3\frac{(2\pi F_x)^2 R_m\left((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim})\right)^2}{C_{t1}(C_{t2} + C_{trim})}$$

Equation 6.5: Transconductance Required for Oscillation

BlueCore6-ROM (WLCSP) guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level required is determined by the crystal driver transconductance.

6.3.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore6-ROM (WLCSP) crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 6.6:

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m (2\pi F_X)^2 (C_0 + C_{int})\left((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim})\right)^2}$$

Equation 6.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore6-ROM (WLCSP) driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (where oscillation occurs) is the equivalent negative resistance of the oscillator.

The BlueCore6-ROM (WLCSP) firmware automatically servos the drive level on the crystal circuit to achieve optimum input swing. The `PSKEY_XTAL_TARGET_AMPLITUDE` (`0x24B`) is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

6.3.5 Crystal PS Key Settings

See Table 6.1.

7 Microcontroller, Memory and Baseband Logic

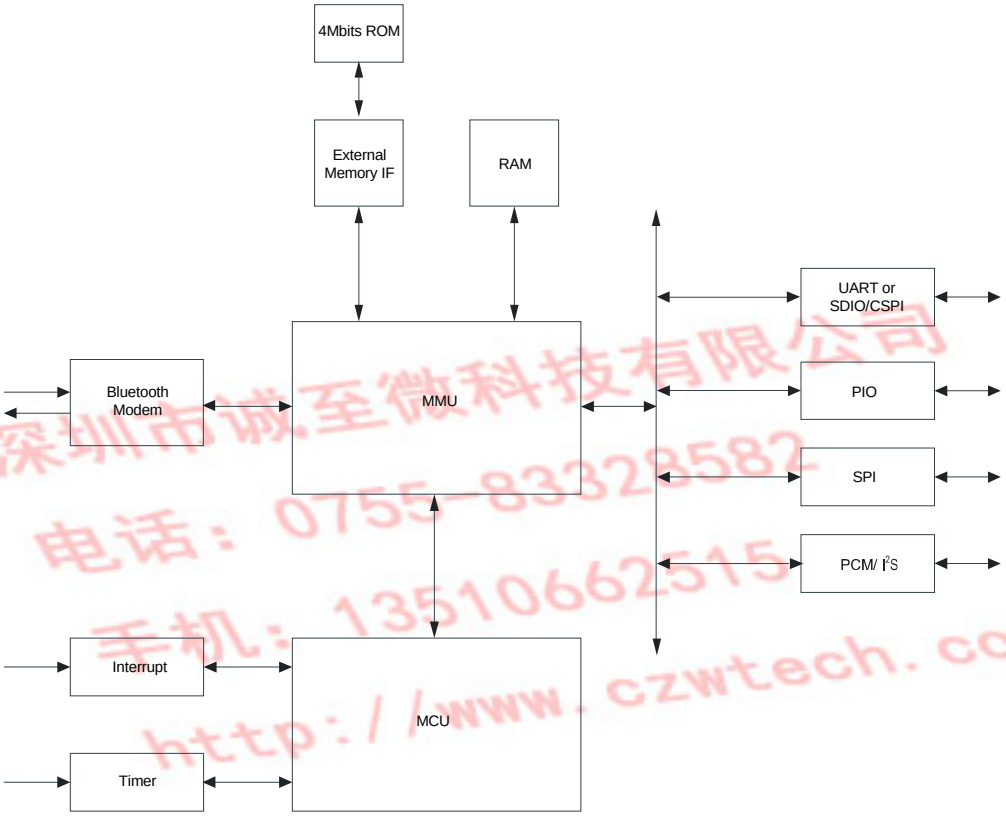


Figure 7.1: Baseband Digits Block Diagram

7.1 AuriStream CODEC

The AuriStream CODEC works on the principle of transmitting the delta between the actual value of the signal and a prediction rather than the signal itself. Hence, the information transmitted is reduced along with the power requirement. The quality of the output depends on the number of bits used to represent the sample.

The inclusion of AuriStream results in reduced power consumption compared to a CVSD implementation when used at both ends of the system.

7.1.1 AuriStream CODEC Requirements

AuriStream supports the following modes of operation:

	fs	Bit Rate (kbps)							
		16	20	24	32	40	48	64	80
G726	8 kHz	(✓)		✓	✓	✓			
	10 kHz				(✓)		(✓)	(✓)	(✓)
G722	8 kHz		(✓)	(✓)	(✓)				
	16 kHz					(✓)	✓	✓	

Table 7.1: AuriStream Supported Bitrates

Table Key:

✓ = Standard Mode

(✓) = Optional Mode

Where possible, AuriStream shares hardware between the encoder and decoder as well as the G726 and G722 implementations of the standard. The 40kbs and 20kbs modes of the G722 CODEC are specific to CSR.

The AuriStream module will be required to support the 3Mbps stream transmitted by the BT radio. The worst-case scenario arises when the AuriStream block is configured as 16kbps at 8 kHz, which equates to 2 bits per sample, giving a worst-case symbol rate at the input to the AuriStream block of 1.5Msps to sustain the transmitted bit stream.

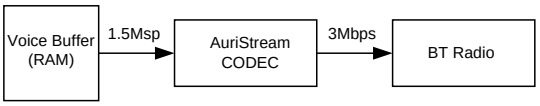


Figure 7.2: AuriStream CODEC and the BT Radio

7.1.2 AuriStream Hierarchy

The AuriStream CODEC is positioned in parallel with the CVSD CODEC as shown in Figure 7.3

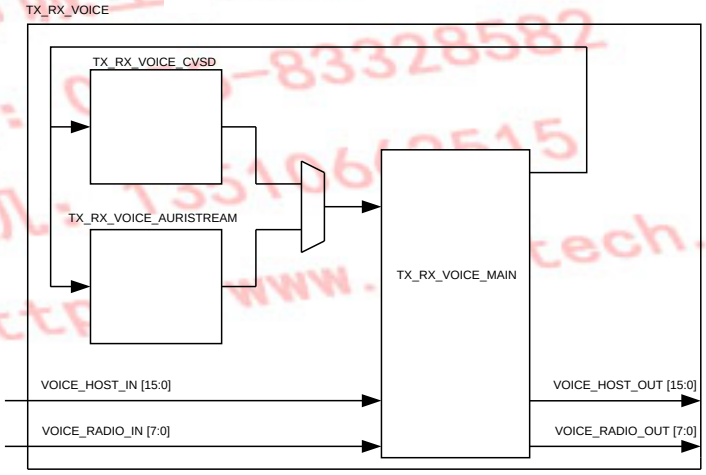


Figure 7.3: AuriStream CODEC and the CVSD CODEC

The AuriStream CODEC is controlled by the `TX_RX_VOICE_MAIN` block and the processor. Raw data from the host is read from the MMU by the transmit block. This data is fed via the `TX_RX_VOICE_MAIN` block to the required CODEC. The encoded data is then fed back to the transmit block for broadcast over the Bluetooth interface. During reception, the data is sourced from the radio and applied to the required CODEC. The decoded data is then stored back to RAM by the bluetooth receiver.

7.2 Memory Management Unit

The *Memory Management Unit* (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available *Random Access Memory*(RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.3 Burst Mode Controller

During transmission the *Burst Mode Controller* (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.4 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/*Continuously Variable Slope Delta* (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR including AFH and eSCO.

7.5 System RAM

48KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.6 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

7.7 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces. A 16-bit *reduced instruction set computer* (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.8 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore6-ROM (WLCSP) where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore6-ROM (WLCSP).

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

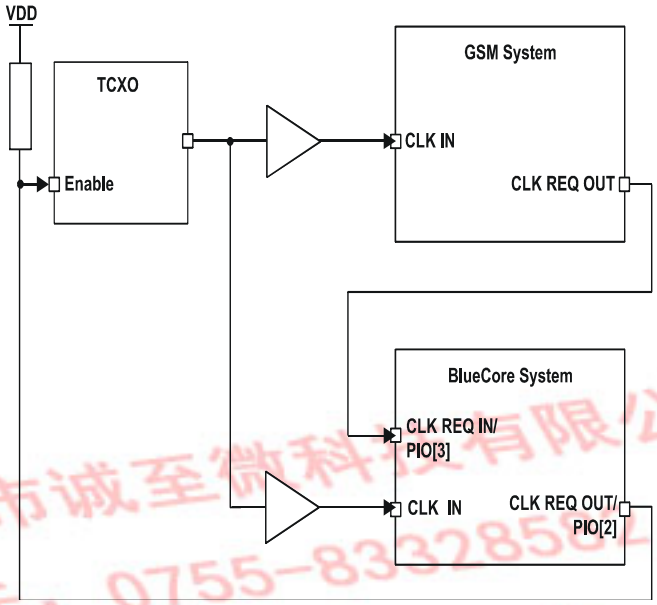


Figure 7.4: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a resistor (470kΩ) to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

7.9 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware.

For more information see *CSR Bluetooth Coexistence Implementations*.

7.10 Configurable I/O Parallel Ports

8 lines of programmable bi-directional *input/outputs* (I/O) are provided. PIO[0: 5, 7, 9] are powered from VDD_PADS. AIO[0] is powered from VDD_ANA.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[2] can be configured as a request line for an external clock source. Using `PSKEY_CLOCK_REQUEST_ENABLE` (`0x246`), this terminal can be configured to be low when BlueCore6-ROM (WLCSP) is in Deep-Sleep and high when a clock is required. See also section 7.8

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

7.11 TX-RX

PIO[0] and PIO[1] are usually dedicated to RXEN and TXEN respectively, but they are also available for general use.

8 Serial Peripheral Interface (SPI)

8.1 BlueCore6-ROM (WLCSP) Serial Peripheral Interface (SPI)

SPI is used for debug primarily. This section details the considerations required when interfacing to BlueCore6-ROM (WLCSP) via the SPI .

Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

8.1.1 Instruction Cycle

The BlueCore6-ROM (WLCSP) is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.1 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 8.1: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore6-ROM (WLCSP) on the rising edge of the clock line SPI_CLK. When reading, BlueCore6-ROM (WLCSP) replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore6-ROM (WLCSP) offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.1.2 Writing to the Device

To write to BlueCore6-ROM (WLCSP), the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

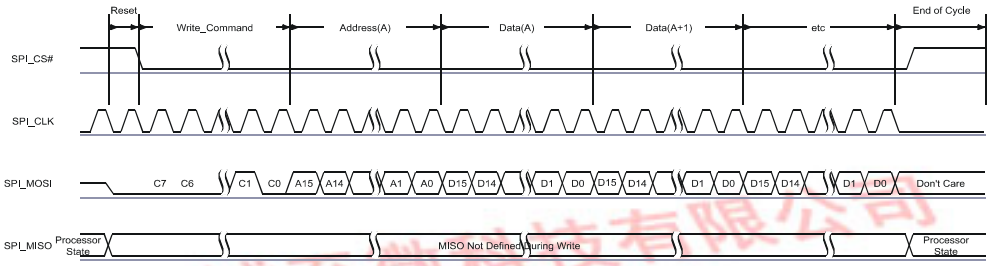


Figure 8.1: SPI Write Operation

8.1.3 Reading from the Device

Reading from BlueCore6-ROM (WLCSP) is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore6-ROM (WLCSP) then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

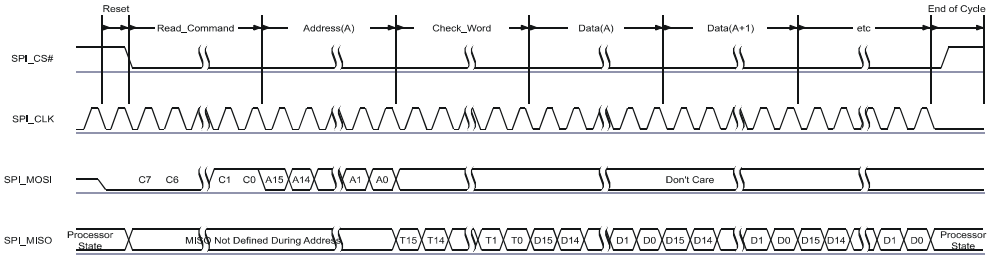


Figure 8.2: SPI Read Operation

8.1.4 Multi-Slave Operation

BlueCore6-ROM (WLCSP) should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore6-ROM (WLCSP) is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore6-ROM (WLCSP) outputs 0 if the processor is running or 1 if it is stopped.

9 Host Interfaces

9.1 Host Selection

The MCU selects the UART/SDIO interfaces by reading PIO[4] at boot-time. When PIO[4] is high, the SDIO interface is enabled; when PIO[4] is low, the UART is enabled.

If in UART mode, the MCU selects the UART transfer protocol automatically using the unused SDIO pins shown in Table 9.1.

SDIO_CLK	SDIO_CMD	Protocol
0	0	bcsp
0	1	h4
1	0	h4ds
1	1	h5

Table 9.1: SDIO_CLK and SDIO_CMD Transfer Protocols

9.2 UART Interface

This is a standard UART interface for communicating with other serial devices.

BlueCore6-ROM (WLCSP) UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.(1)

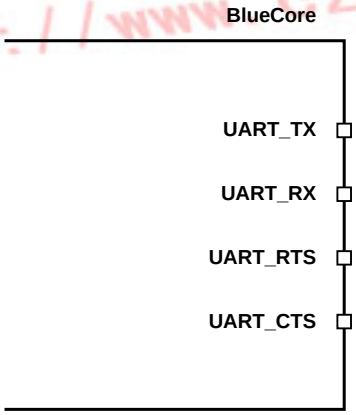


Figure 9.1: Universal Asynchronous Receiver

Four signals implement the UART function, as shown in Figure 9.1. When BlueCore6-ROM (WLCSP) is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore6-ROM (WLCSP) firmware.

Note:

An accelerated serial port adapter card is required to communicate with the UART at maximum baud rate using a standard PC.

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_PADS (requires external RS232 transceiver chip).

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 9.2: Possible UART Settings

Note:

Baud rate is the measure of symbol rate, i.e., the number of distinct symbol changes (signalling events) made to the transmission medium per second in a digitally modulated signal. See also Section 17

The UART interface is capable of resetting BlueCore6-ROM (WLCSP) on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Table 9.2. If t_{BRK} is longer than the value, defined by the `PSKEY_HOSTIO_UART_RESET_TIMEOUT`, (`0x1a4`), a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore6-ROM (WLCSP) can emit a break character that may be used to wake the host.

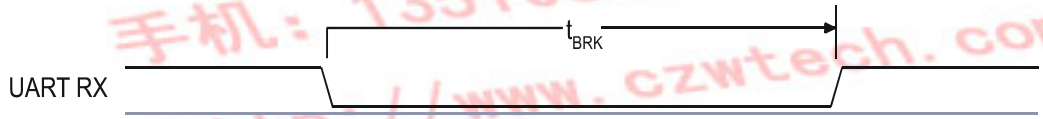


Figure 9.2: Break Signal

Table 9.3 shows a list of commonly used baud rates and their associated values for the `PSKEY_UART_BAUDRATE` (`0x1be`). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 9.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 9.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 9.3: Standard Baud Rates

9.2.1 UART Configuration While Reset is Active

The UART interface for BlueCore6-ROM (WLCSP) is tri-state while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore6-ROM (WLCSP) reset is de-asserted and the firmware begins to run.

9.3 CSR Serial Peripheral Interface (CSPI)

The CSPI is a host interface which shares pins with the SDIO. It has been defined by CSR with the intention of producing a very simple interface. This has two advantages:

- It allows maximum compatibility with the possible host drivers
- It minimises the host software effort needed to form that data to be sent (e.g., by removing the need to calculate CRCs)

This host interface allows an external host to control the Bluecore, using a CSR defined protocol built upon a 4-wire SPI bus.

Note:

The CSPI is entirely separate from the debug Serial Peripheral Interface described in Section 8.

CSPI allows access to the following:

- Function 0 registers
- Bluetooth Acceleration Registers
- MCU IO Registers
- Bluetooth MMU port

The CSPI is a third protocol available for the host to transfer data into the Bluecore and shares pins with the other SDIO protocols.

MMU buffers are accessed using burst read/writes. The command and address fields are used to select the correct buffer. The CSPI is able to generate an interrupt to the host when a memory access fails. This interrupt line is shared with the SDIO functions.

Table 9.4 shows the mapping of SDIO pins onto the CSPI functions when CSPI is enabled.

Pin	CSPI Function	Direction	Description
SDIO_DATA3	CSB	I	Chip Select
SDIO_CMD	MOSI	I	Master Out Slave In
SDIO_DATA0	MISO	O	Master In Slave Out
SDIO_CLK	CLK	I	Clock
SDIO_DATA1	INT	O	Interrupt

Table 9.4: SDIO Mapping to CSPI Functions

The CSPI Interface is an extension of the basic SPI Interface, with the access type determined by the following fields:

- 8-bit command (to initiate CSPI read/write access)
- 24-bit address
- 16-bit burst length (optional). Only applicable for burst transfers into or out of the MMU

9.3.1 CSPI Read/Write Cycles

Register read/write cycles are used to access Function 0, Bluetooth acceleration and MCU registers.

Burst read/write cycles are used to access the MMU.

9.3.2 CSPI Register Write Cycle

The command and address are locked into the slave, followed by 16bits of write data. An Error Byte is returned on the MISO signal indicating whether or not the transfer has been successful.

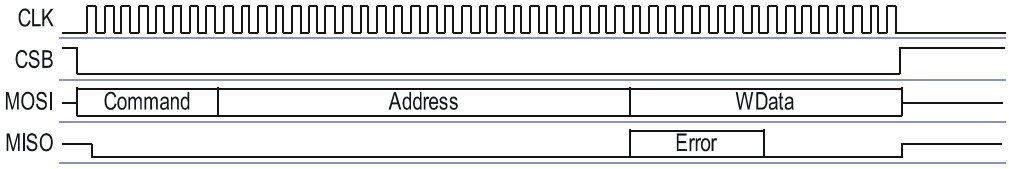


Figure 9.3: CSPI Register Write Cycle

9.3.3 CSPI Register Read Cycle

The command and address field are clocked into the slave, the slave then returns the following:

- Bytes of Padding data (MISO held low)
- Error Byte
- 16-bits of read data

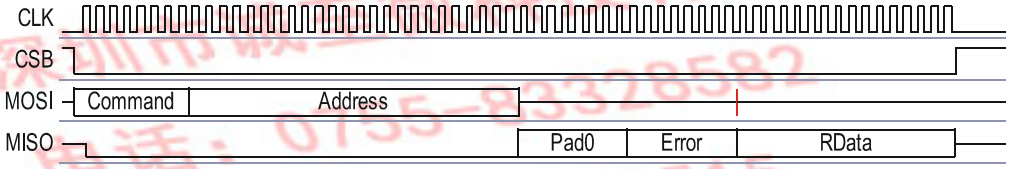


Figure 9.4: CSPI Register Read Cycle

9.3.4 CSPI Burst Write Cycle

Burst transfers are used to access the MMU buffers. They cannot be used to access registers. Burst read/write cycles are selected by setting the `nRegister/Burst` bit in the command field to `1`.

Burst transfers are byte orientated, have a minimum length of 0 bytes and a maximum length of 64kbytes. Setting the length field to `0` results in no data being transferred to or from the MMU.

As with a register access, the command and address fields are transferred first. There is an optional length field transferred after the address. The use of the length field is controlled by the `LengthFieldPresent` bit in the Function 0 registers, which is cleared on reset.

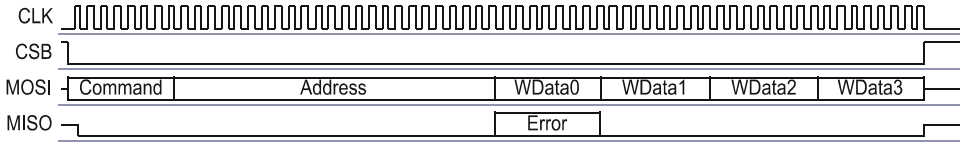


Figure 9.5: CSPI Burst Write Cycle

9.3.5 CSPI Burst Read Cycle

Burst reads have a programmable amount of padding data that is returned by the slave. 0-15 bytes are returned as defined in the `BurstPadding` register. Following this the Error byte is returned followed by the data. Once the transfer has started, no further padding is needed.

A FIFO within `SDIO_TOP` will pre-fetch the data. The address is not retransmitted, and is auto-updated within the slave.

The length field is transmitted if `LengthFieldPresent`in the Function 0 registers is set. In the absence of a length field the CSB signal is used to indicate the end of the burst.

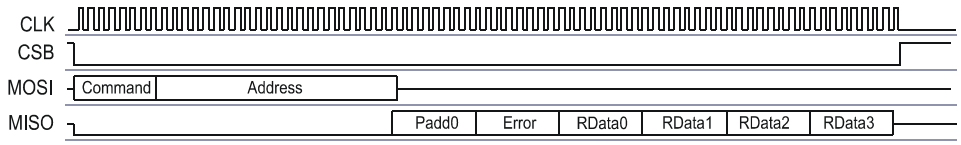


Figure 9.6: CSPI Burst Read Cycle

9.4 SDIO Interface

This is a host interface which allows a *Secure Digital Input Output* (SDIO) host to gain access to the internals of the chip. It provides all defined slave modes (SPI, SD 1bit, SD 4bit), but not SD host function.

The function provided includes generating responses to each command in hardware and implementing the state machines defined in the SDIO specification. Within the various modes of operation, it provides initialisation functions (`cmds 0,3,5,7,15,59`) and two other functions:

- Function 1 provides Bluetooth type A support, and follows that specification
- Function 2 provides generic register access (`cmd52` (byte read/write))

For more information, see the following specifications:

- *SD Specifications Part 1 Physical layer specification v1.10*
- *SD Specifications Part E1 SDIO specification v1.10*
- *SDIO Card Part E2 Type-A Specification for Bluetooth v1.00*

9.4.1 SDIO/CSPI Deep-Sleep Control Schemes

This is the lowest power mode, where the processor, the internal reference (fast) clock, and much of the digital and analogue hardware are shut down. To support this power consumption reduction solution and to prevent any errors arising on the SDIO host interface there are two Deep-Sleep control schemes.

- *Scheme 1:* The host retransmits any packets that Bluecore was unable to receive as a result of being in Deep-Sleep.
- *Scheme 2:* Introduces additional signaling to prevent the need for retransmissions

During Deep-Sleep the internal reference clock is turned off. However, the host transport protocols (SDIO/UART/CSPI) are driven from the SDIO clock and so continue to function during Deep-Sleep, enabling access to the function 0 interface, but not the function 1 interface.

9.4.2 Retransmission

Bluecore enters Deep-Sleep whenever it becomes idle after which time, when the host transmits a message on function 1 an illegal command error will be signaled. The activity that this initiates on the SDIO Interface provokes Bluecore into wakeup after which the host re-transmits the original message.

Bluecore will wait for a configurable period of time before re-entering Deep-Sleep, thus ensuring that the original packet is sent/received on retransmission. This control scheme is the default mode of operation.

9.4.3 Signalling

Signalling between the host and Bluecore enables host control over Bluecore Deep-Sleep mode. Consequently the host is aware of when it is appropriate to send Bluecore HCI traffic over function 1.

The signals used by this scheme are *Host wakeup* and *Ready status interrupt select*, implemented as register bit in the vendor unique area of function 0.

10 Audio Interfaces

10.1 PCM Interface

The audio *Pulse Code Modulation* (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore6-ROM (WLCSP) has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore6-ROM (WLCSP) offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore6-ROM (WLCSP) allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore6-ROM (WLCSP) can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz. When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz. BlueCore6-ROM (WLCSP) is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting `PSKEY_PCM_CONFIG32` (`0x1b3`).

BlueCore6-ROM (WLCSP) interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and µ-law CODEC
- Motorola MC145481 8-bit A-law and µ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore6-ROM (WLCSP) is also compatible with the Motorola SSI interface

10.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore6-ROM (WLCSP) generates PCM_CLK and PCM_SYNC.

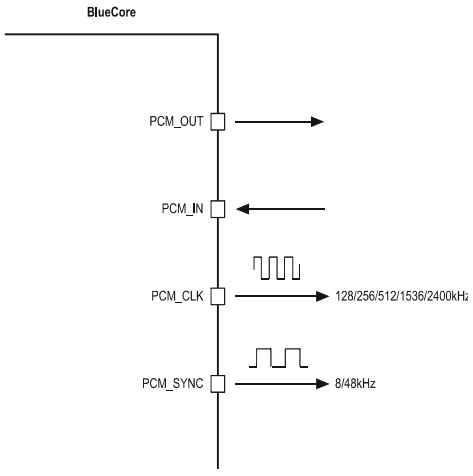


Figure 10.1: BlueCore6-ROM (WLCSP) as PCM Interface Master

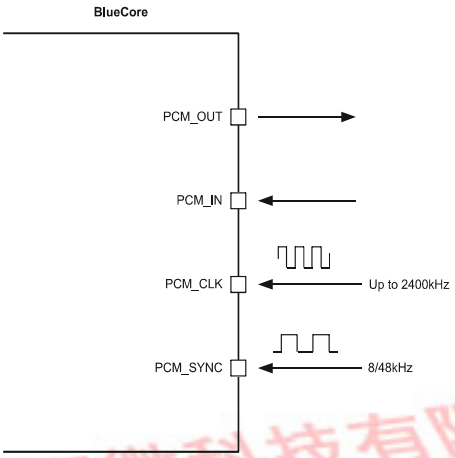


Figure 10.2: BlueCore6-ROM (WLCSP) as PCM Interface Slave

10.1.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore6-ROM (WLCSP) is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore6-ROM (WLCSP) is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

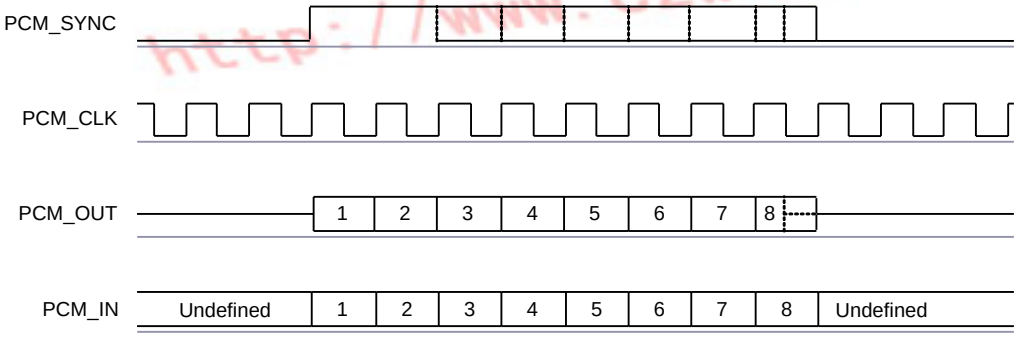


Figure 10.3: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore6-ROM (WLCSP) samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.1.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

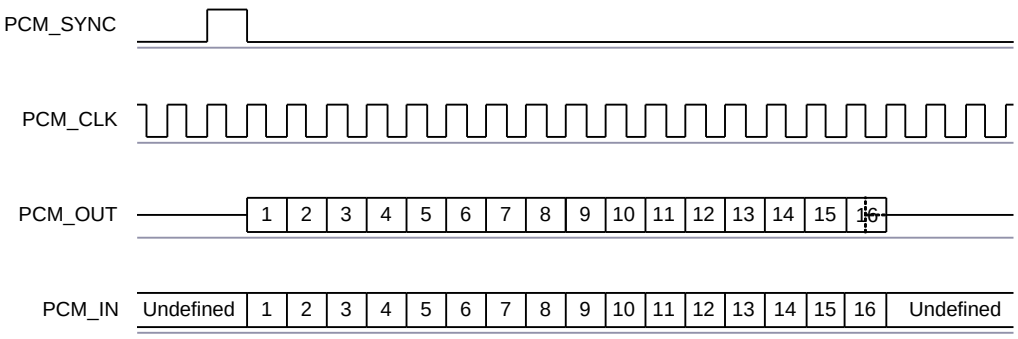


Figure 10.4: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore6-ROM (WLCSP) samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.1.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

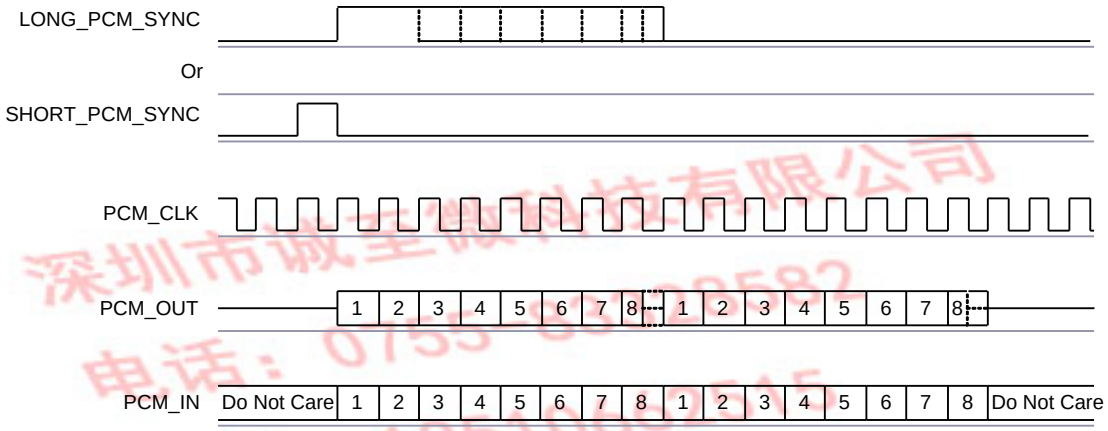


Figure 10.5: Multi-slot Operation with Two Slots and 8-bit Companded Samples

10.1.5 GCI Interface

BlueCore6-ROM (WLCSP) is compatible with the *General Circuit Interface* (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

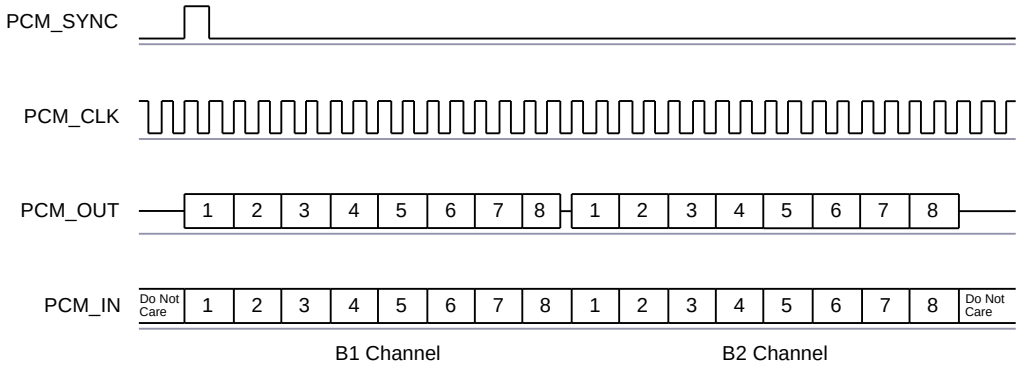


Figure 10.6: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore6-ROM (WLCSP) in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

10.1.6 Slots and Sample Formats

BlueCore6-ROM (WLCSP) can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore6-ROM (WLCSP) supports 13-bit linear, 16-bit linear and 8-bit µ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

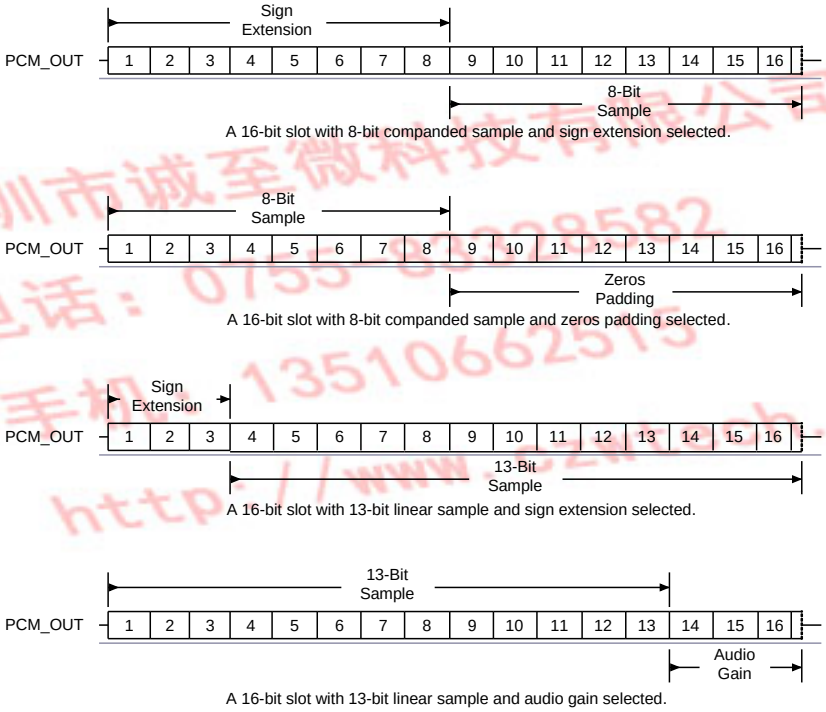


Figure 10.7: 16-Bit Slot Length and Sample Formats

10.1.7 Additional Features

BlueCore6-ROM (WLCSP) has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

10.1.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 10.4.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable. See Table 10.3 and section 10.1.9.	2.9	-	-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 10.1: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

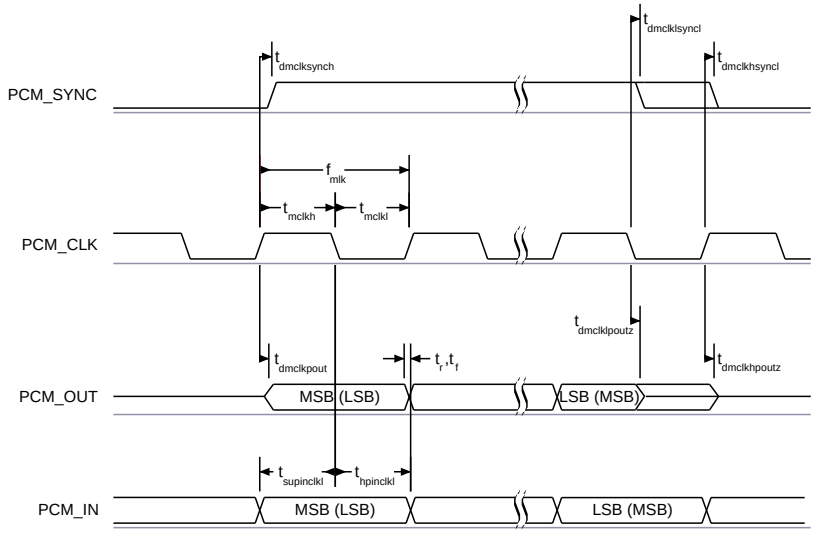


Figure 10.8: PCM Master Timing Long Frame Sync

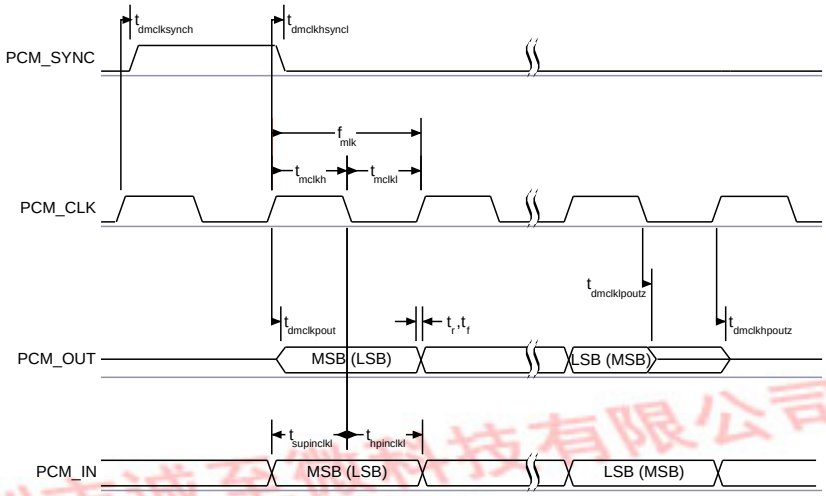


Figure 10.9: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 10.2: PCM Slave Timing

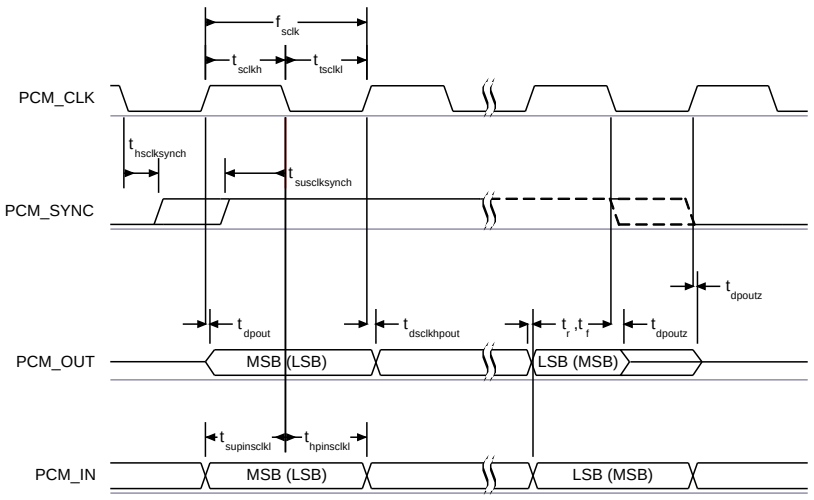


Figure 10.10: PCM Slave Timing Long Frame Sync

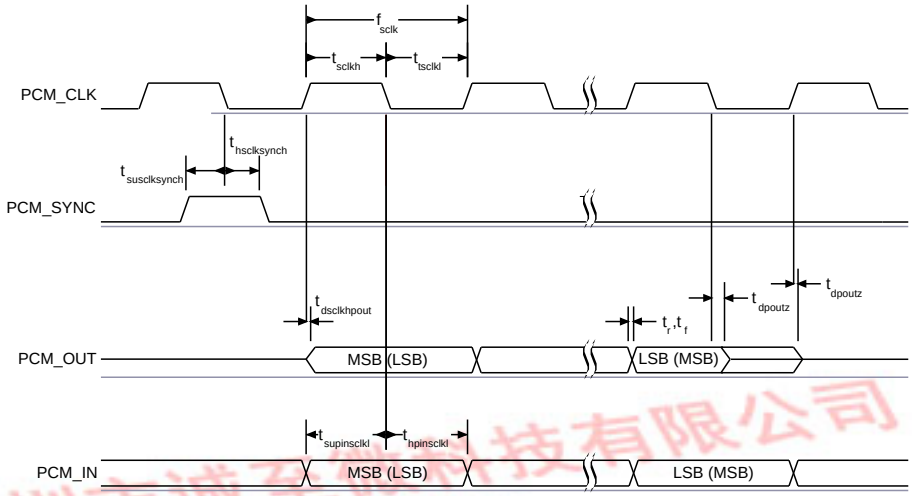


Figure 10.11: PCM Slave Timing Short Frame Sync

10.1.9 PCM_CLK and PCM_SYNC Generation

BlueCore6-ROM (WLCSP) has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by *Direct Digital Synthesis* (DDS) from BlueCore6-ROM (WLCSP) internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit `48M_PCM_CLK_GEN_EN` in `PSKEY_PCM_CONFIG32`. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by `LONG_LENGTH_SYNC_EN` in `PSKEY_PCM_CONFIG32`.

Equation 10.1 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 10.1: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 10.2 dependent on the setting of `PCM_SYNC_MULT` (see Table 10.5). If set:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT} \qquad f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 10.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using `PSKEY_PCM_LOW_JITTER_CONFIG`. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set `PSKEY_PCM_LOW_JITTER_CONFIG` to `0x08080177`.

10.1.10 PCM Configuration

The PCM configuration is set using the PS Keys, `PSKEY_PCM_CONFIG32` described in Table 10.4, `PSKEY_PCM_LOW_JITTER_CONFIG` in Table 10.3, and `PSKEY_PCM_SYNC_MULT` in Table 10.5. The default for `PSKEY_PCM_CONFIG32`is `0x00800000`, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 10.3: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode
MUTE_EN	10	1 = force PCM_OUT to 0
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN(bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 10.4: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
PCM_SYNC_MULT	12	0 - Sync limit = SYNC_LIMIT x 8 1 - SYNC_LIMIT

Table 10.5: PSKEY_PCM_SYNC_MULT Description

10.2 Digital Audio Interface (I^2S)

The digital audio interface supports the industry standard formats for I^2S, left-justified (LJ) or right-justified(RJ). The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 10.6 lists these alternative functions. Figure 10.12 shows the timing diagram.

PCM Interface	I^2S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 10.6: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 10.7 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I^2S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6dB steps
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1only the most significant 16 bits of data are received

Table 10.7: PSKEY_DIGITAL_AUDIO_CONFIG

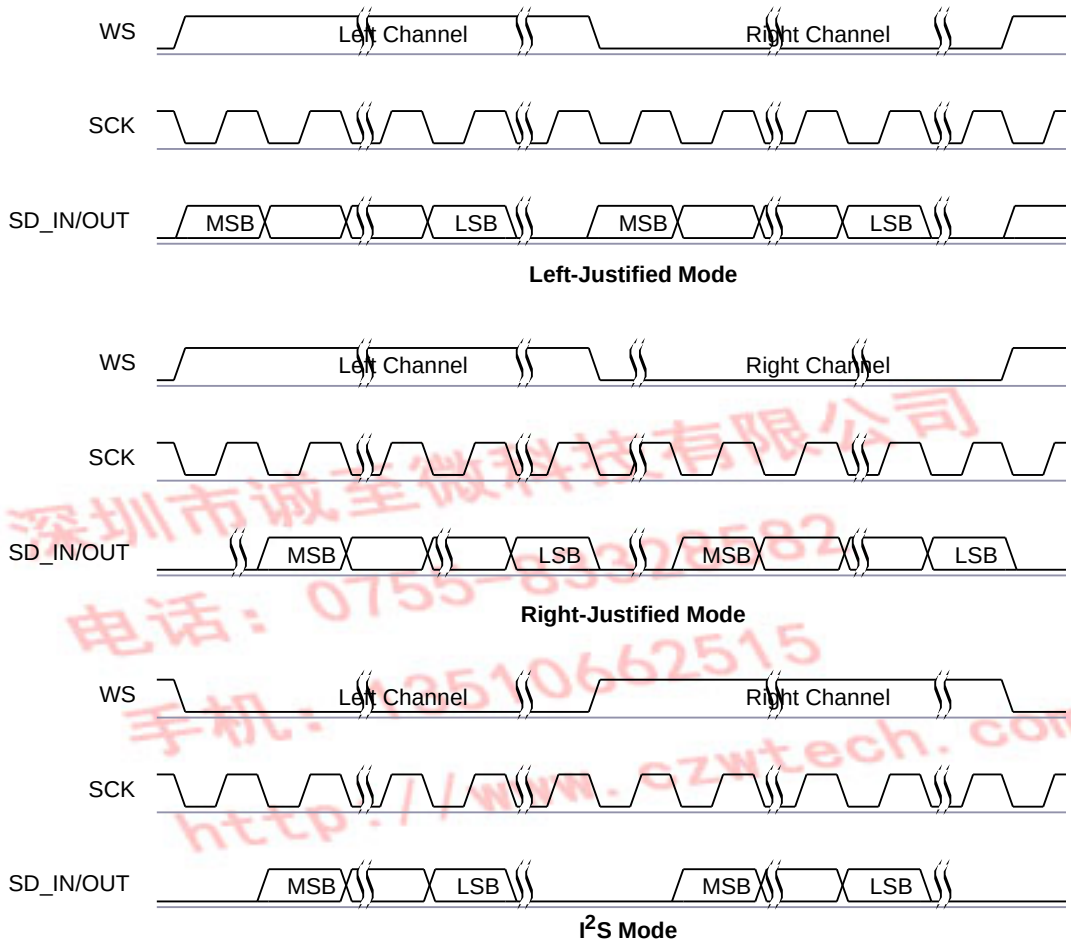


Figure 10.12: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore6-ROM (WLCSP) is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 10.8: Digital Audio Interface Slave Timing

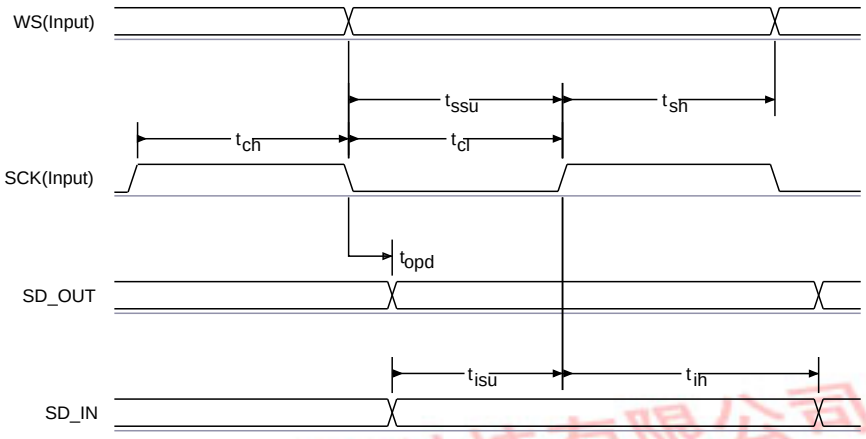


Figure 10.13: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 10.9: Digital Audio Interface Master Timing

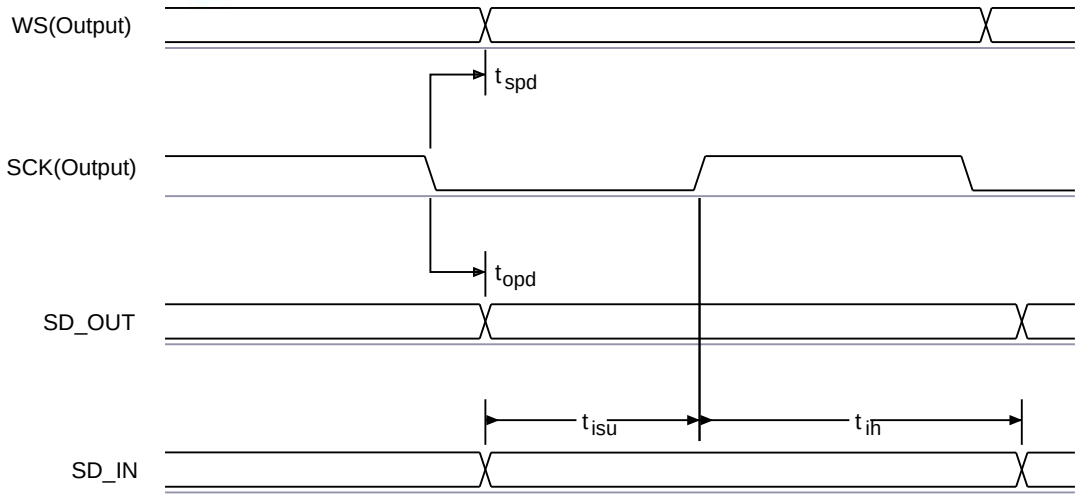


Figure 10.14: Digital Audio Interface Master Timing

11 Power Control and Regulation

11.1 Power Control and Regulation

BlueCore6-ROM (WLCSP) contains two linear regulators:

- A high voltage regulator to generate a 1.8V rail for the chip I/Os
- A low-voltage regulator to supply the 1.5V core supplies from the 1.8V rail.

The chip can be powered from a high-voltage rail through both regulators. Alternatively the chip can be powered directly from an external 1.8V rail, bypassing the high- voltage regulator, or from an external 1.5V rail omitting both regulators.

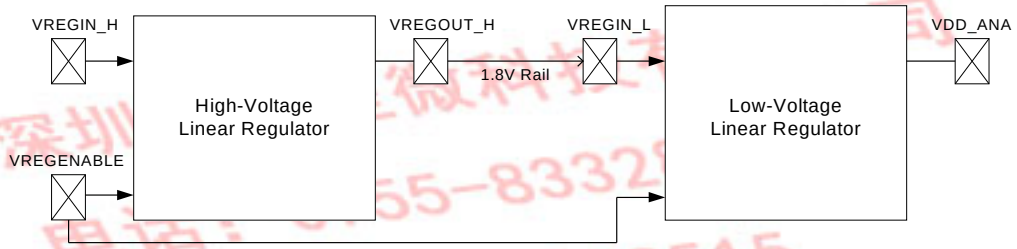


Figure 11.1: Voltage Regulator Configuration

11.2 Sequencing

The 1.5V supplies are VDD_ANA, VDD_RADIO and VDD_CORE. It is recommended that the 1.5V supplies are all powered at the same time.

The order of powering the 1.5V supplies relative to the other I/O supply (VDD_PADS) is not important. However, if the I/O supply is powered before the 1.5V supplies the digital pads default to their No Core Voltage Reset state. VDD_ANA and VDD_RADIO should be connected directly to the 1.5V supply; a simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

11.3 External Voltage Source

If the 1.5V rails of BlueCore6-ROM (WLCSP) are supplied from an external voltage source, it is recommended that VDD_RADIO and VDD_ANA should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels (refer to the average current consumption specification of the regulator).

11.4 High-Voltage Linear Regulator

The on-chip high-voltage regulator may be used to power the 1.8V rail. A smoothing circuit using a low ESR capacitor (2.2µF) and a resistor to ground (2.2Ω), should be connected to on the output of the regulator VREGOUT_H. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The regulator may be enabled by the VREGENABLE pin, by the device firmware, or by the internal battery charger.

The regulator is switched into a low power mode when the device is in Deep-Sleep mode, or in reset.

When this regulator is not used the terminals VREGIN_H and VREGOUT_H must be left unconnected, or tied to ground.

11.5 Low-Voltage Linear Regulator

The on-chip low-voltage regulator may be used to power all the chip 1.5V supplies. The output of this regulator is connected internally to VDD_ANA, and must be connected externally to the other 1.5V supply pads. A smoothing circuit using a low ESR capacitor (2.2µF) and a resistor (2.2Ω) to ground should be connected to the output of the regulator. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω. See the example Application Schematic in Section 12.

This regulator may be enabled by the VREGENABLE pin, by the device firmware, or by the internal battery charger.

The regulator is switched into a low power mode when the device is in Deep-Sleep mode, or in reset.

When this regulator is not used the terminal VREGIN_L must be left unconnected, or tied to VDD_ANA.

11.6 VREGENABLE

The regulator enable pin VREGENABLE is used to enable and disable the BlueCore6-ROM (WLCSP) device if the on-chip regulators are being used. VREGENABLE enables both the high voltage regulator and the low voltage regulator.

The pin is active high, with a logic threshold of around 1V, and has a weak pull-down to the input of the regulators it controls.

The status of the VREGENABLE pin is available to firmware through an internal connection.

11.7 RST#

BlueCore6-ROM (WLCSP) may be reset from several sources: RST# pin, power on reset, a UART break character or via a software configured watchdog timer.

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. It is recommended that RST# be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.24V and is released when VDD_CORE rises above typically 1.31V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown in Table 11.1. Following a reset, BlueCore6-ROM (WLCSP) assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore6-ROM (WLCSP) is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore6-ROM (WLCSP) free runs, again at a safe frequency.

11.7.1 Digital Pin States on Reset

The digital I/O interfaces on the BlueCore6-ROM (WLCSP) device are optimised for minimum power consumption after initialisation of digital interfaces.

Table 11.1 shows the pin states of BlueCore6-ROM (WLCSP) on reset. `Pull-up` (PU) and `pull-down` (PD) default to weak values unless specified otherwise.

Pin Name/Group	I/O Type	No Core Voltage Reset		Full Chip Reset	
		Pull R	I/O	Pull R	I/O
Reset/Control					
RST#	Digital input	PU	Input	PU	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Digital Interfaces - SDIO					
SDIO_DATA[3]	Digital bi-directional	PD	Input	PU	Input
SDIO_DATA[2]	Digital bi-directional	PD	Input	PU	Input
SDIO_DATA[1]	Digital bi-directional	PD	Input	PU	Input
SDIO_DATA[0]	Digital bi-directional	PD	Input	PU	Input

Pin Name/Group	I/O Type	No Core Voltage Reset		Full Chip Reset	
		Pull R	I/O	Pull R	I/O
SDIO_SD_CS#	Digital bi-directional	PD	Input	PU	Input
SDIO_CMD	Digital bi-directional	PD	Input	PU	Input
SDIO_CLK	Digital bi-directional	PD	Input	PU	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
PCM Interface					
PCM_IN	Digital input	PD	Input	PD	Input
PCM_OUT	Digital tri-state output	PD	High impedance	PD	High impedance
PCM_CLK	Digital bi-directional	PD	Input	PD	Input
PCM_SYNC	Digital bi-directional	PD	Input	PD	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
SPI Interface					
SPI_MOSI	Digital input	PD	Input	PD	Input
SPI_CLK	Digital input	PD	Input	PD	Input
SPI_CS#	Digital input	PU	Input	PU	Input
SPI_MISO	Digital tri-state output	PD	High impedance	PD	High impedance
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
PIOs					
PIO[0]	Digital bi-directional	PD	Input	PD	Input
PIO[1]	Digital bi-directional	PD	Input	PD	Input
PIO[2]	Digital bi-directional	PD	Input	PD	Input
PIO[3]	Digital bi-directional	PD	Input	PD	Input
PIO[4]	Digital bi-directional	PD	Input	PD	Input
PIO[5]	Digital bi-directional	PD	Input	PD	Input
PIO[7]	Digital bi-directional	PD	Input	PD	Input
PIO[9]	Digital bi-directional	PD	Input	PD	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Clocks					
XTAL_IN	Ref clock	None	Input	None	Input
CLK_32K	Digital input	PD	Input	PD	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Test					
TEST_EN	Digital input	Strong PD	Input	Strong PD	Input

Table 11.1: Pin States of BlueCore6-ROM (WLCSP) on Reset

12 Example Application Schematic

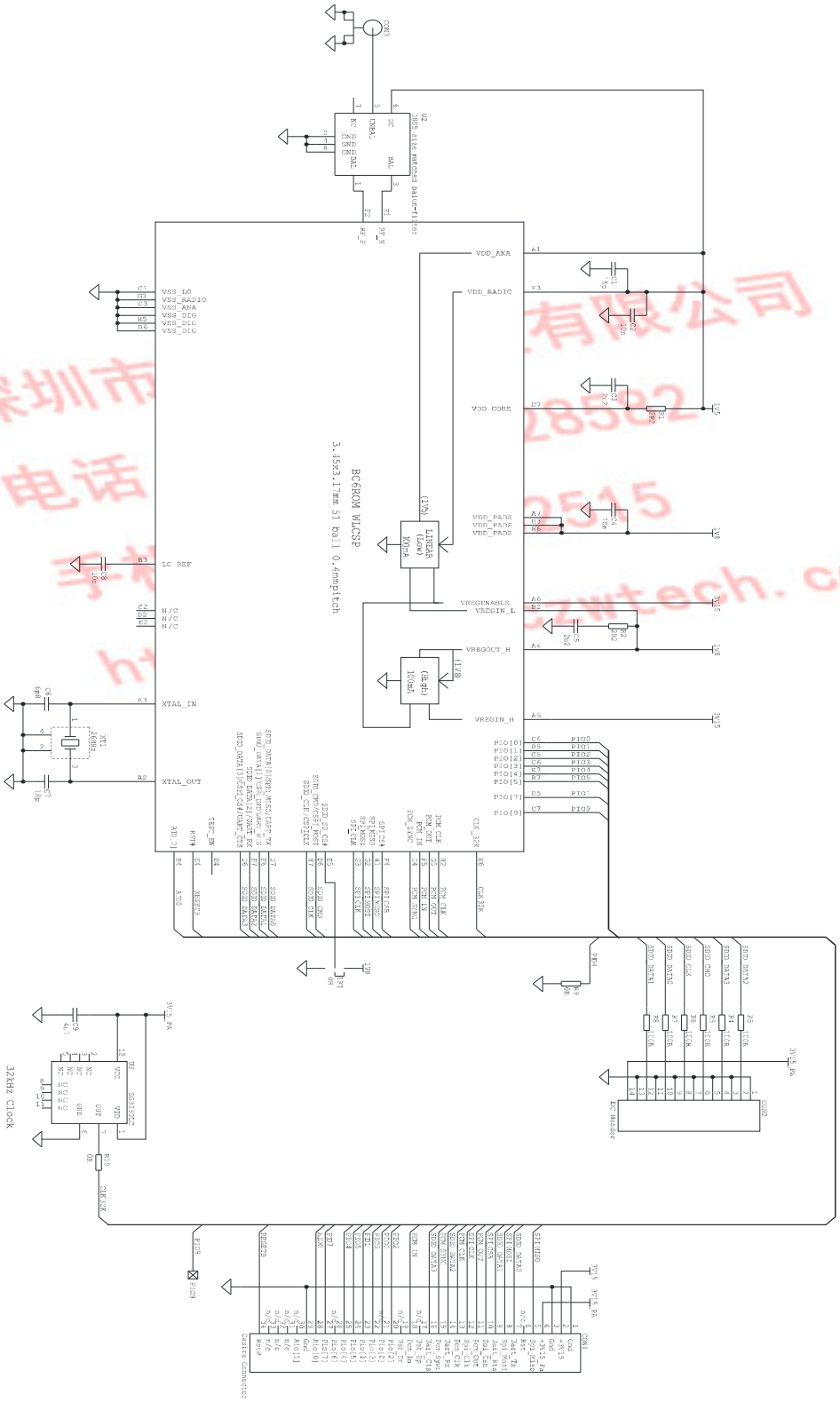


Figure 12.1: Example Application Schematic

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	+85	°C
Core Supply Voltage	VDD_RADIO, VDD_ANA and VDD_CORE	-0.4	1.65	V
IO Voltage	VDD_PADS	-0.4	3.7	V
Supply Voltage	VREGIN_L	-0.4	2.7	V
	VREGIN_H, VREGENABLE	-0.4	4.9	V
Other Terminal Voltages		VSS-0.4	VDD+0.4	V

13.2 Recommended Operating Conditions

Operating Condition		Min	Max	Unit
Operating Temperature Range		-40	+85	°C
Core Supply Voltage	VDD_RADIO, VDD_ANA and VDD_CORE	1.4	1.6	V
IO Voltage	VDD_PADS	1.7	1.9	V

13.3 Input/Output Terminal Characteristics

Notes:

VDD_CORE, VDD_RADIO and VDD_ANA are at 1.5V unless shown otherwise.

VDD_PADS is at 1.8V unless shown otherwise.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

13.3.1 Linear Regulator, High Voltage

Normal Operation	**Min**	**Typ**	**Max**	**Unit**
Input Voltage	2.5	-	5.5[a]	V
Output Voltage (I_{load} = 100mA / VREGIN_H = 3.0V)	1.70	1.80	1.9	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[b][c]	-	-	1	mV rms
Load Regulation (I_{load} < 100mA)	-	-	50	mV/A
Settling Time[b][d]	-	-	50	µs
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Dropout Voltage (I_{load} = 100mA)	-	-	600	mV
Quiescent Current (excluding load, I_{load} < 1mA)	30	40	60	µA
Low Power Mode[e]				
Quiescent Current (excluding load, I_{load} < 100µA)	10	13	21	µA
Standby Mode[f]				
Quiescent Current	1.5	2.5	3.5	µA

(a) Operation up to 5.5V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore6-ROM (WLCSP), but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.9V. 5.5V can only be tolerated for short periods.

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range is 100Hz to 100kHz.

(d) 1mA to 100mA pulsed load.

(e) Low power mode is entered and exited automatically when the chip enters/leaves Deep-Sleep mode.

(f) Regulator is in standby when VREGENABLE is pulled low.

13.3.2 Linear Regulator, Low Voltage

Normal Operation	Min	Typ	Max	Unit
Input Voltage	1.7	-	2.7	V
Output Voltage[a] (I_{load} = 100mA / VREGIN_H = 1.7V)	1.4	1.5	1.6	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[b][c]	-	-	1	mV rms
Load Regulation (I_{load} < 100mA)	-	-	50	mV/A
Settling Time[b][d]	-	-	50	µs
Maximum Output Current	70	-	-	mA
Minimum Load Current	5	-	-	µA
Dropout Voltage (I_{load} = 100mA)	-	-	200	mV
Quiescent Current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low Power Mode[e]				
Quiescent Current (excluding load, I_{load} < 100µA)	6	10	17	µA
Standby Mode[f]				
Quiescent Current	1.5	2.5	3.5	µA

(a) For optimum performance, the VDD_ANA Ball adjacent to VREGIN_H should be used for regulator output,

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range is 100Hz to 100kHz.

(d) 1mA to 100mA pulsed load.

(e) Low power mode is entered and exited automatically when the chip enters/leaves Deep-Sleep mode.

(f) Regulator is in standby when VREGENABLE is pulled low. It is also in standby when VREGIN_L is either open circuit or driven to the same voltage as VDD_ANA.

13.3.3 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low 1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V	-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V	VDD-0.4	-	-	V
Input and Tri-state Current with:				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	+10	+40	+100	µA
Weak pull-up	-5.0	-1.0	-0.2	µA
Weak pull-down	+0.2	+1.0	+5.0	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input capacitance	1.0	-	5.0	pF

13.3.4 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	16.0	26.0	26.0	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
Clock Source	**Min**	**Typ**	**Max**	**Unit**
External Clock				
Input frequency[a]	12	-	52.0	MHz
Clock input level[b]	0.4	-	VDD_ANA	V pk-pk
Allowable jitter	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

(a) Integer multiple of 250kHz

(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(a) Clock input can be any frequency between 12MHz and 52MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(b) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

13.3.5 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.24	1.30	V
VDD_CORE rising threshold	1.20	1.31	1.35	V
Hysteresis	0.05	0.07	0.15	V

13.3.6 RSSI ADC

RSSI ADC[a]		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range (LSB size = VDD_ANA/1024)		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	+1	LSB
	DNL	0	-	1	LSB
Offset		-4	-	+4	LSB
Gain Error		-0.2	-	0.2	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.75	-	µs
Sample rate		-	-	700	Samples/s

[a] For more information about this ADC, see section 5.2.2

13.3.7 External Reference Clock

Parameter	Conditions/ Notes	Specification			Units
		Min	Nom	Max	
Frequency		32748	32768	32788	Hz
Frequency deviation	@25°C	-	-	20	±ppm
Frequency deviation	-20°C to 85°C	-	-	150	±ppm
Input high level	Square wave	0.625 x VDD_PADS	-	-	V
Input low level	Square wave	-	-	0.425 x VDD_PADS	V
Duty cycle	Square wave	30	-	70	%
Rise and fall time		-	-	50	ns
Integrated frequency jitter	Integrated over the band 200Hz to 15kHz	-	-	-	Hz (rms)

13.4 Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval 1.28s	-	0.8	mA
ACL no traffic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1.28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 - hands-free - setting S1	Master	18.5	mA
SCO HV1	Master	37	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	µA
Reset (active low)	-	39	µA

Note:

Conditions: 20°C, VREGIN_H 3.15V

VDD_PADS: 3.15V

UART BAUD rate: 115.2kbps

Typical Peak Current @ +20°C	
Device Activity/State	**Current (mA)**
Peak current during cold boot	45
Peak TX current Master	45
Peak RX current Master	40
Peak TX current Slave	45
Peak RX current Slave	45
Conditions	
Firmware	HCI 22 (provisionally)
VREGIN_H, VDD_PADS	3.15
Host Interfaces	UART
UART Baud rate	115200
Clock source	26MHz crystal
RF output power	0dBm

14 CSR Software Stacks

BC63B239A04 is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

14.1 BlueCore HCI Stack

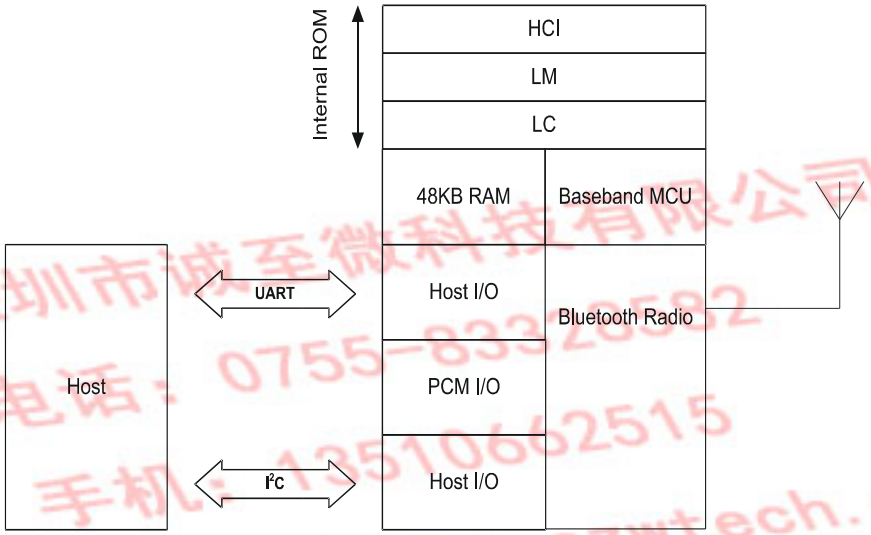


Figure 14.1: BlueCore HCI Stack

In the implementation shown in section 14.1 the internal processor runs the Bluetooth stack up to the *Host Controller Interface* (HCI). The Host processor must provide all upper layers including the application.

14.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

Bluetooth v2.1 + EDR mandatory functionality:

- *Adaptive frequency hopping* (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.1 + EDR functionality supported:

- *Adaptive Frequency Hopping* (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- *Extended SCO* (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(2)
- Operation with up to seven active slaves(2)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(3)
- Maximum number of simultaneous active SCO connections: 3(3)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard *Protocol Implementation Conformance Statement* (PICS) documents, available from http://www.csr.com.

(2) This is the maximum allowed by Bluetooth v2.1 + EDR specification.

(3) BlueCore6-ROM (WLCSP) supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification.

14.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports *BlueCore Serial Protocol* (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting Deep-Sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called *BlueCore Command* (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the chip's *Persistent Store* (PS) configuration database. The database sets the device's Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, constants, etc.
- A UART break condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep-Sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: Shallow Sleep and Deep-Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's PCM ports (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

14.2 BCHS Software

BlueCore Embedded Host Software (BCHS) is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies), SDIO, SPI
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

14.3 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore6-ROM (WLCSP), a UART software driver is supplied that presents the L2CAP, RFCOMM and `Service Discovery Protocol` (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

14.4 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore6-ROM (WLCSP) hardware and software, and as toolkits for developing on-chip and host software.

15 Ordering Information

15.1 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART	51 ball WLCSP (Pb free)	3.21 x 3.49 x 0.6mm (max.), 0.4mm pitch	Tape and reel	BC63B239A04-IYB-E4[a]

[a] Until BC63B239A04 reaches **Production** status, order number is BC63B239A04-ES-IYB-E4

Minimum Order Quantity

2kpcs taped and reeled

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

15.2 Tape and Reel Information

For tape and reel packing and labeling see *IC Packing and Labelling Specification*.

16 Document References

Document:	Reference, Date:
Specification of the Bluetooth System	v2.1 + EDR, 31 July 2007
CSR Bluetooth Coexistence Implementations	CS-110632-AN
BCCMD Commands	CS-101482-SPP (bcore-sp-005P)
HQ Commands	CS-101677-SPP (bcore-sp-003P)
IC Packing and Labelling Specification	CS-112584-SPP
SD Specifications Part 1 Physical layer specification v1.10	For more information, see http://www.sdcard.org/sdio/index.html
SD Specifications Part E1 SDIO specification v1.10	
SDIO Card Part E2 Type-A Specification for Bluetooth v1.00	

17 Terms and Definitions

Term	Definition
2KPCS	2000 pieces
3G	3rd Generation of Multimedia
8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
ACL	Asynchronous Connection-Less. Bluetooth data packet
ADC	Analogue to Digital Converter
ADPCM	Adaptive Differential Pulse code Modulation
AFC	Automatic Frequency Control
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIO	Asynchronous Input/Output
A-law	Audio encoding standard
AM	Amplitude Modulation
ANSI	American National Standards Institute
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
AuriStream	CSR proprietary ADPCM CODEC
BAF	Audio Frequency Band
balun	A device that connects a balanced line to an unbalanced line; for example, a twisted pair to a coaxial cable
Baud	Baud rate is the measure of symbol rate, i.e., the number of distinct symbol changes (signalling events) made to the transmission medium per second in a digitally modulated signal
BCCMD	BlueCore™ Command
BCSP	BlueCore Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
BW	Band Width
CDMA	Code Division Multiple Access
C/I	Carrier-to-cochannel interference ratio
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CRC	Cyclic Redundancy Check
CS	Channel Separation
CS#	Chip Select (Active Low)
CSPI	CSR Serial Peripheral Interface
CSR	Cambridge Silicon Radio
CTS	Clear to Send

Term	Definition
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DDS	Direct Digital Synthesis
DEVM	Differential Error Vector Magnitude
DNL	Differential Non-Linearity
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quarternary Phase Shift Keying
DSP	Digital Signal Processor
EDR	Enhanced Data Rate
eSCO	extended SCO
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
FHS	Frequency Hopping Synchronization
FIFO	First In First Out
FSK	Frequency Shift Keying
GCI	General Circuit Interface
GND	Ground
GPS	Global Positioning System
GSM	Global System for Mobile communications
H4	UART-based HCI transport, described in section H4 of v1.0b of Bluetooth Specification
H4DS	H4 Deep-Sleep
HCI	Host Controller Interface
HQ	Host Query
I^2S	Inter-Interchip Circuit Sound
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
I/O	Input/Output
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
KB	Kilobyte. See kbyte
kbyte	In this context, a kilobyte is a unit of memory chip capacity equal to 1,024 bytes. It is also abbreviated KB
kbps	Kilobit per second. A unit of data transfer rate equal to 1,000 bits per second
ksps	KiloSamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LED	Light Emitting Diode
LJ	Left Justified

Term	Definition
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
µ-law	Audio Encoding Standard
Mbaud	Mega baud
Mbits	Mega bits
Mbps	Mega bits per second
MCU	MicroController Unit
MMU	Memory Management Unit
MISO	Master In Serial Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
OHCI	Open Host Controller Interface
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PD	Pull-Down
PDA	Personal Digital Assistant
PICS	Protocol Implementation Confirmation Statement or Profile Implementation Confirmation Statement (both are used)
PIO	Parallel Input Output
Pk-Pk	Peak-to-Peak
PLL	Phase Lock Loop
ppm	parts per million
PS	Persistent Store
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
PU	Pull-Up
RAM	Random Access Memory
RC	Resistor Capacitor
RDS	Radio Data System
RE#	Read enable (Active Low)
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RJ	Right Justified
RL	Load Resistance
rms	root mean squared
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)

Term	Definition
ROM	Read-Only Memory
RS232	Recommended Standard 232. A TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Receive Signal Strength Indication
RST#	Reset pin for test and debug
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDP	Service Discovery Protocol
SNR	Signal Noise Ratio
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TBA	To Be Announced
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion + Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
VDD	This is the positive power supply for the chip. V refers to Voltage. The double letters (DD) refer to 'drain' voltage
VSS	This is the ground power supply for the chip. V refers to Voltage. The double letters (SS) refer to 'source' voltage
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access
WCS	Wireless Coexistence System
WE#	Write Enable (Active Low)
WLAN	Wireless Local Area Network
WLCSP	Wafer-Level Chip Scale Package
XTAL	Crystal

18 Document History

Revision	Date	History
1	14 MAY 07	Original publication of this document
2	24 AUG 07	Update for Bluetooth v2.1 + EDR and AuriStream
3	05 SEPT 07	Package dimensions and product/order number updated. Document Feedback section added

18.1 Document Feedback

If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.