Features

- Fully qualified Bluetooth® v2.1 + EDR Specification
- Qualified for Class 2 operation
- Piconet and scatternet support
- Minimum external components
- Low-power 1.5V operation, 1.8V to 3.6V I/O
- Integrated 1.5V regulator
- UART to 4Mbaud
- Integrated CSR AuriStream® low-power codec for wide-band voice quality
- 3.21 x 3.49 x 0.6mm (max.), 0.5mm-pitch WLCSP
- Support for 802.11 coexistence
- Green (RoHS and no antimony or halogenated flame retardants)
- AuriStream (16, 24, 32, 40 kbps) codec offering significant power reduction over the CVSD-based system

BlueCore®6-ROM

Single-chip Bluetooth v2.1 + EDR System

Production Information

BC6888A04

Issue 10

BlueCore6-ROM 0.5mm-pitch WLCSP Data Sheet

General Description

BlueCore®6-ROM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbps.

With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth v2.1 + EDR specification system for data and voice communications.

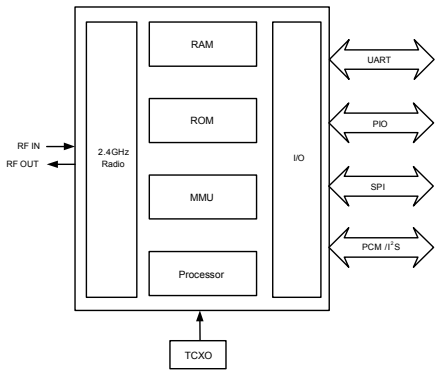

Figure: System Architecture

Applications

- Cellular handsets
- PDAs
- PNDs

BlueCore6-ROM has been designed to reduce the number of external components required which ensures production costs are minimised.

BlueCore6-ROM includes AuriStream, which offers significant power reduction over the CVSD-based system when used at both ends of the link.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification.

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of coexistence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

Device Details

Bluetooth Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- No external trimming is required in production
- Bluetooth v2.1 + EDR Specification compliant

Bluetooth Transmitter

- +9dBm maximum RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Qualified for Class 2 operation

Bluetooth Receiver

- Receiver sensitivity of -90dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with an external clock between 12 and 52MHz

Baseband and Software

- AuriStream (16, 24, 32, 40 kbps) codec offering significant power reduction over the CVSD-based system when used at both ends of the link
- Internal 48kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.1 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- SPI interface up to 4Mbits/s for system debugging
- UART interface with programmable data rate up to 4Mbaud
- Bi-directional serial programmable audio interface supporting PCM and I^2S formats

Auxiliary Features

- Clock request output to control an external clock
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Auto Baud Rate setting, subject to host interface in use
- On-chip low dropout linear regulator producing 1.5V core voltage from 1.8V
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in the configuration:

- Standard HCI over UART

Package Options

- 33-ball 3.21 x 3.49 x 0.6mm (max.), 0.5mm-pitch WLCSP

Device Diagram

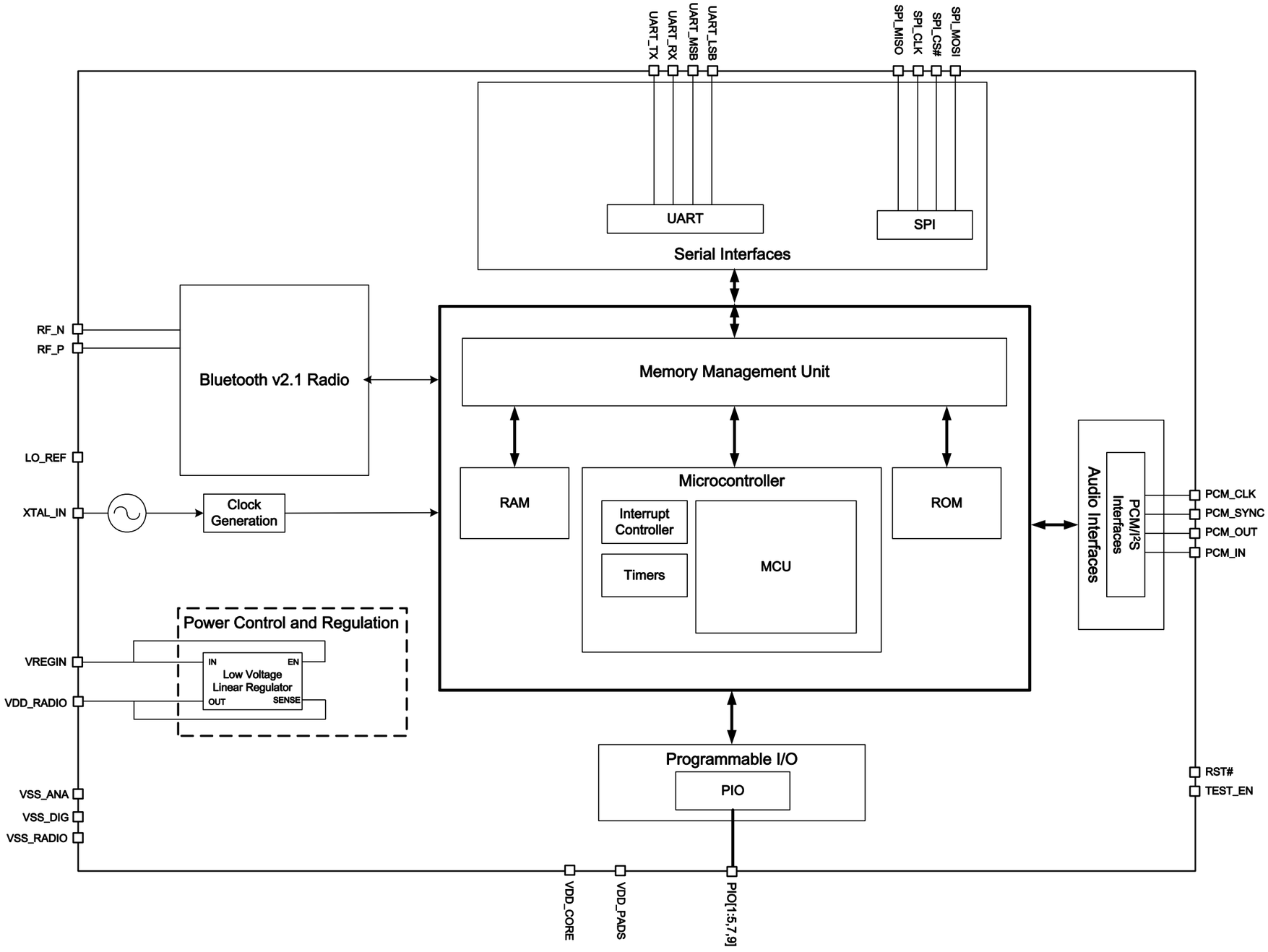

Figure : Device Diagram

Document History

Revision	Date	Change Reason
1	28 OCT 08	Original publication of this document.
2	31 OCT 08	Updated pinout information and device diagram, and added schematic.
3	07 NOV 08	Text corrections.
4	18 NOV 08	Updated Package Dimensions graphic.
5	31 DEC 08	Further update to Package Dimensions graphic. Updated System Architecture diagram. Updated schematic. Text corrections.
6	09 JAN 09	Updated tape and reel information. Added host transport selection information.
7	20 MAR 09	Updated TX and RX sensitivities. Editorial updates throughout.
8	09 APR 09	Editorial updates.
9	18 JUN 09	ROM size corrected. Host Selection section updated.
10	14 JUL 09	Section 6.1 updated. Section 8 corrected. Updated to Production Information status. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Product Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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Contents

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1 Package Information

1.1 Device Pinout

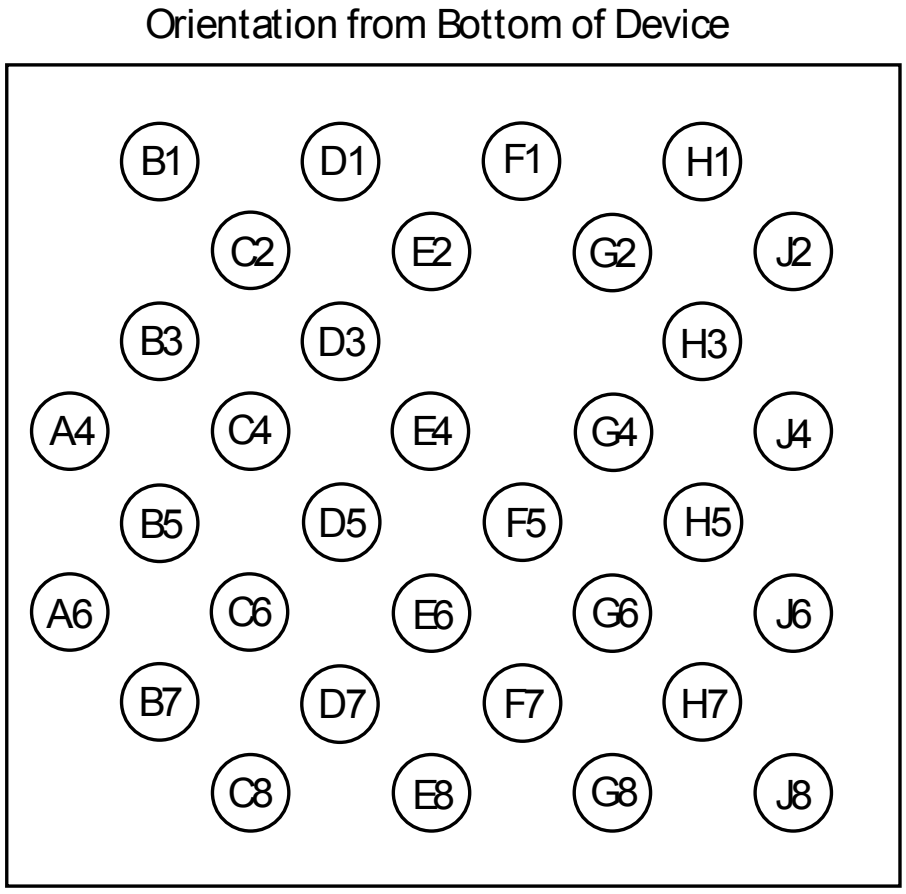


Figure 1.1: BlueCore6-ROM Device Pinout

1.2 Device Terminal Functions

Bluetooth Radio	Ball	Pad Type	Supply Domain	Description
RF_N	D1	RF	VDD_RADIO	Transmitter output/switched receiver input
RF_P	F1	RF	VDD_RADIO	Complement of RF_N

Synthesiser and Oscillator	Ball	Pad Type	Supply Domain	Description
XTAL_IN	A4	Analogue	VDD_RADIO	For TCXO external clock input
LO_REF	B3	Analogue	VDD_RADIO	Reference voltage decoupling

SPI Interface	Ball	Pad Type	Supply Domain	Description
SPI_MOSI	H1	Input with weak internal pull-down	VDD_PADS	SPI data input
SPI_CS#	G4	Input with weak internal pull-up	VDD_PADS	Chip select for SPI, active low
SPI_CLK	E4	Input with weak internal pull-down	VDD_PADS	SPI clock
SPI_MISO	C4	Output, tri-state, with weak internal pull-down	VDD_PADS	SPI data output

UART Interface	Ball	Pad Type	Supply Domain	Description
UART_TX	G8	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	UART data output, active high
UART_RX	J8	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	UART data input, active high
UART_LSB	H7	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	UART protocol select
UART_MSB	F7	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	UART protocol select

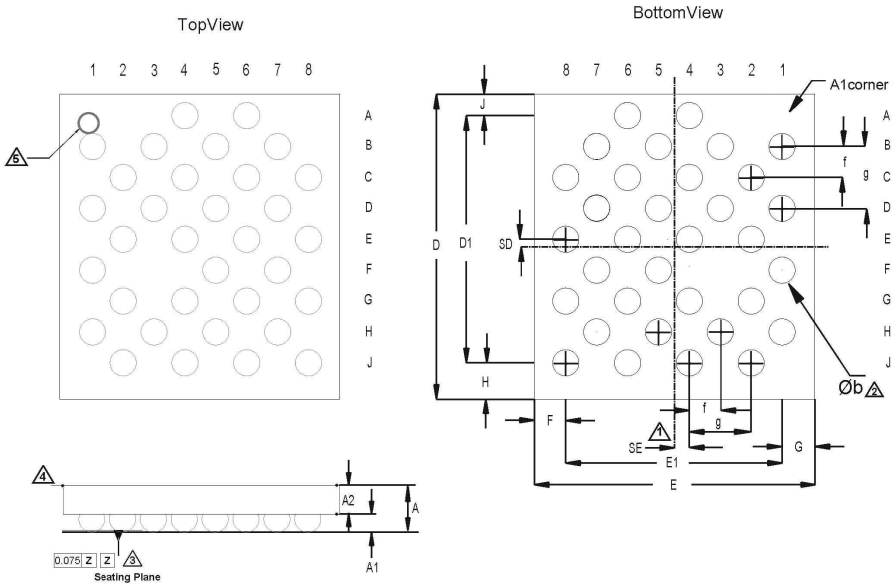
PCM Interface	Ball	Pad Type	Supply Domain	Description
PCM_OUT	J2	Output, tri-state, with weak internal pull-down	VDD_PADS	Synchronous data output
PCM_IN	F5	Input, with weak internal pull-down	VDD_PADS	Synchronous data input
PCM_SYNC	H5	Bi-directional with weak internal pull-down	VDD_PADS	Synchronous data sync
PCM_CLK	J4	Bi-directional with weak internal pull-down	VDD_PADS	Synchronous data clock

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[9]	E8	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[7]	D7	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[5]	G6	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[4]	E6	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[3]	B7	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[2]	C6	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[1]	D5	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[0]	B5	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line

Test and Debug	Ball	Pad Type	Supply Domain	Description
RST#	D3	Input with weak internal pull-up	VDD_PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	H3	Input with strong internal pull-down	VDD_PADS	For test purposes only (leave unconnected)

Power Supplies	Ball	Description
VREGIN	B1	Take high to enable and power low-voltage regulator
VDD_PADS	J6	Positive supply for digital input/output ports including PIO [9, 7, 5:0]
VDD_CORE	C8	Positive supply for internal digital circuitry
VDD_RADIO	E2	Positive supply for RF circuitry and analogue circuitry. Output from internal 1.5V regulator.
VSS_ANA	C2	Ground connections for analogue circuitry, VCO and synthesiser
VSS_RADIO	G2	Ground connection for RF circuitry
VSS_DIG	A6	Ground connections for digital I/O circuitry

1.3 Package Dimensions



Description	33-ball Wafer-Level Chip Scale Package (WLCSP)			
Size	3.21 x 3.49 x 0.6mm (max)			
Package Ball Land	300µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.54	0.57	0.60	1 Midpoint of ball array is offset to centre of component
A1	0.21	0.24	0.27	
A2		0.33		2 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
b		0.32		
D	3.39	3.44	3.49	
E	3.11	3.16	3.21	3 Datum Z is defined by the spherical crowns of the solder balls
D1		2.828		
E1		2.4745		4 Parallelism measurement shall exclude any effect of mark on top surface of package
f		0.3535		
g		0.707		
F	0.310	0.335	0.360	5 Topside-polarity mark. The dimensions of the polarity mark are 0.3mm diameter.
G	0.3255	0.3505	0.3755	
H	0.367	0.392	0.417	
J	0.195	0.220	0.245	
SD		0.086		
SE		0.169		
JEDEC	Non JEDEC			
Unit	mm			

Figure 1.2: BlueCore6-ROM Package Dimensions

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 3.21 x 3.49 x 0.6mm WLCSP 33-ball package:

- NSMD lands (that is, lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be used to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the RF requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be 300µm ±10µm to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process, because this adds to the final volume of solder in the joint, increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5µm to prevent brittle gold/tin intermetallics forming in the solder.
- The WLCSP is designed so that ball lands do not lie on top of sensitive areas of the active silicon
- WLCSP components often have the ball array mid-point offset to the centre of the component outline. This requires careful consideration during component PCB footprint design.

2 Bluetooth Modem

2.1 RF Ports

2.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

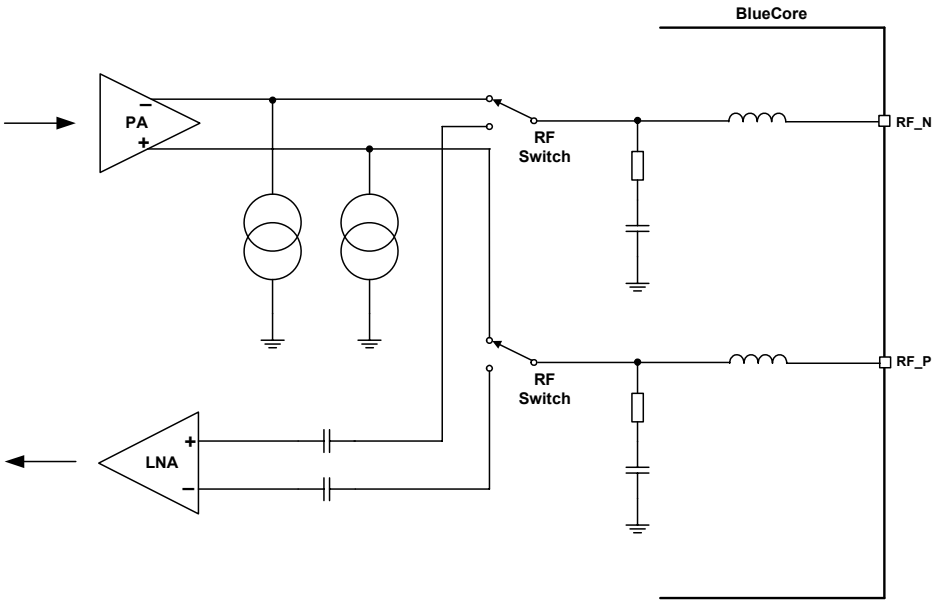


Figure 2.1: Simplified Circuit RF_N and RF_P

The DC level must be set at VDD_RADIO.

2.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore6-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA has a maximum output power that allows BlueCore6-ROM to be used in Class 2 and Class 3 radios without an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

2.6 AuriStream Codec

The AuriStream codec is an ADPCM codec and works on the principle of transmitting the difference between the actual value of the signal and a prediction rather than the signal itself. Therefore, the information transmitted is reduced along with the power requirement. The quality of the output depends on the number of bits used to represent the sample.

Note:

The use of the AuriStream codec is as follows:

- The AuriStream codec is an alternative to standard CVSD
- It requires CSR devices supporting AuriStream at both ends of the link
- AuriStream is negotiated when the link is brought up. If AuriStream is not supported on either end, the system will switch to standard CVSD ensuring full interoperability with any non-AuriStream Bluetooth devices

The inclusion of the AuriStream codec can greatly enhance audio quality in the wideband mode and results in reduced power consumption compared to a CVSD implementation when used at both ends of the system.

AuriStream supports the G726 mode of operation shown in Table 2.1.

fs	Bit-rate (kbps)						
	16	20	24	32	48	64	80
8kHz	✓		✓	✓			
16kHz				✓	✓	✓	✓

Table 2.1: AuriStream Supported Bit-rates for G726

3 Clock Generation

BlueCore6-ROM requires a Bluetooth reference clock. This can be an external TCXO source.

All BlueCore6-ROM internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the external reference clock source.

Also supplied to the digits is a watchdog clock, for use in low power modes. This uses an internally generated reference clock frequency of 1kHz.

The use of the watchdog clock is determined with respect to Bluetooth operation in low power modes.

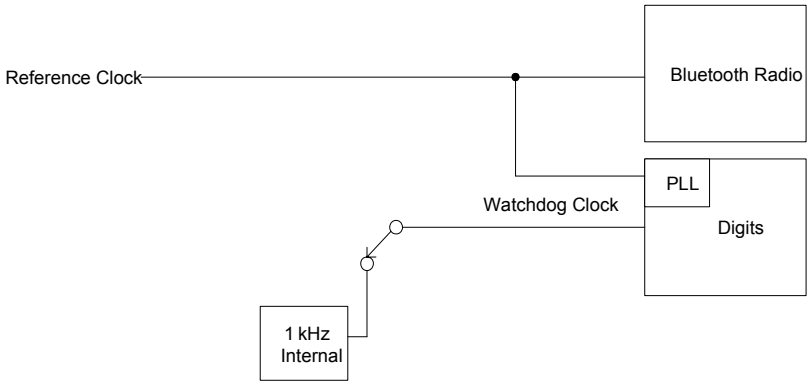


Figure 3.1: Clock Architecture

3.1 Input Frequencies and PS Key Settings

BlueCore6-ROM should be configured to operate with the chosen reference frequency. Do this by setting the PS Key ANA_FREQ (0x01FE) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore6-ROM is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	ANA_FREQ (0x1fe) (kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 0.25	n x 250
26.00 (default)	26000

Table 3.1: PS Key Values for CDMA/3G Phone TCXO

3.2 Clock Start-up Delay

BlueCore6-ROM hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore6-ROM firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1-31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore6-ROM as low as possible. BlueCore6-ROM consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

4 Bluetooth Stack Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

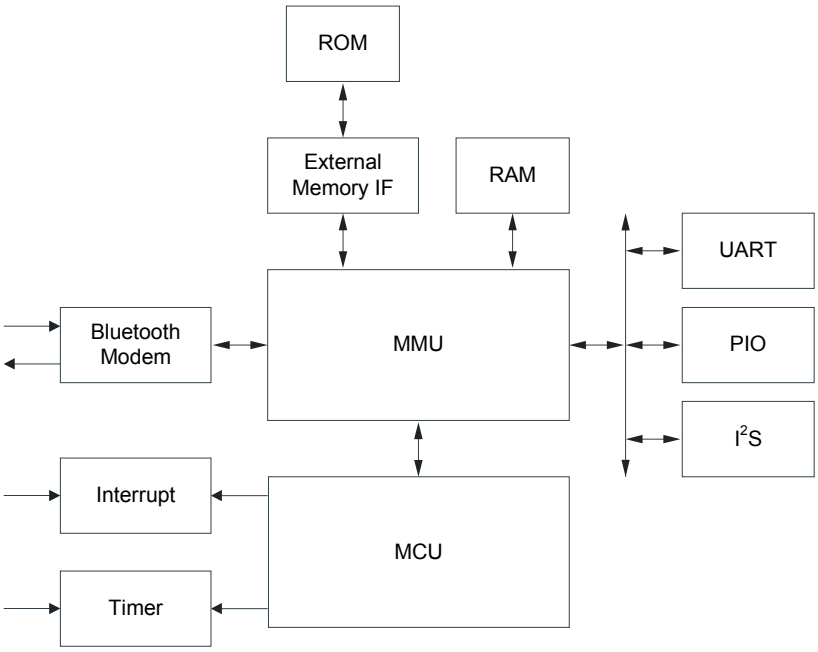


Figure 4.1: Baseband Digits Block Diagram

The on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

4.1 Configurable I/O Parallel Ports

8 lines of programmable bi-directional I/Os are provided. PIO[0: 5, 7, 9] are powered from VDD_PADS.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[2] can be configured as a request line for an external clock source. Using `PSKEY_CLOCK_REQUEST_ENABLE` (`0x246`), this terminal can be configured to be low when BlueCore6-ROM is in Deep-Sleep and high when a clock is required. See also Section 4.2.

Note:

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

4.2 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore6-ROM where either device can turn on the clock without having to wake up the other device, see Figure 4.2. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore6-ROM.

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

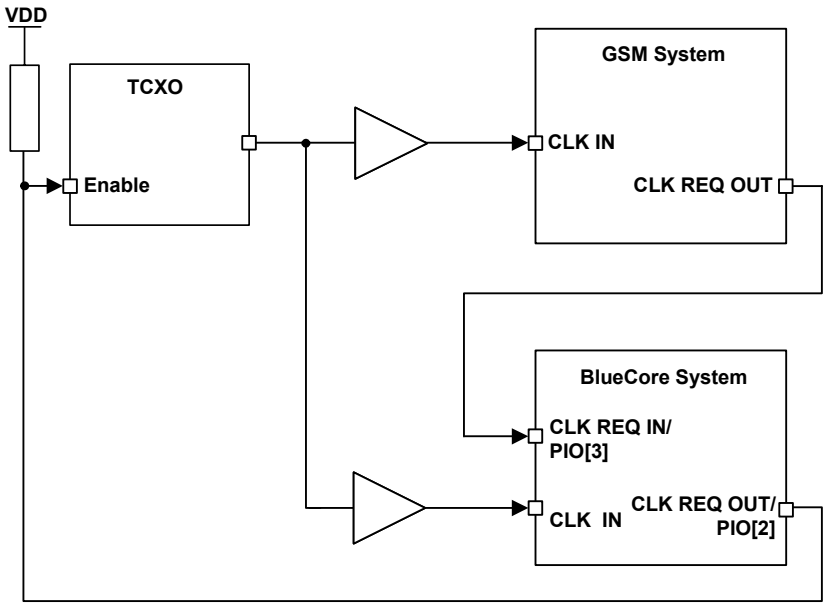


Figure 4.2: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

4.3 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware using PS Keys or via the host.

For more information see *CSR Bluetooth Coexistence Implementations*.

4.4 TX-RX

PIO[0] and PIO[1] are usually dedicated to RXEN and TXEN respectively, but they are also available for general use.

5 Serial Interfaces

5.1 Serial Peripheral Interface

The primary function of the SPI is for debug. BlueCore6-ROM uses a 16-bit data and 16-bit address SPI, where transactions may occur when the internal processor is running or is stopped. This section details the interface considerations for connection to BlueCore6-ROM .

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

5.1.1 Instruction Cycle

The BlueCore6-ROM is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 5.1 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 5.1: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore6-ROM on the rising edge of the clock line SPI_CLK. When reading, BlueCore6-ROM replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore6-ROM offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

5.1.2 Writing to the Device

To write to BlueCore6-ROM, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

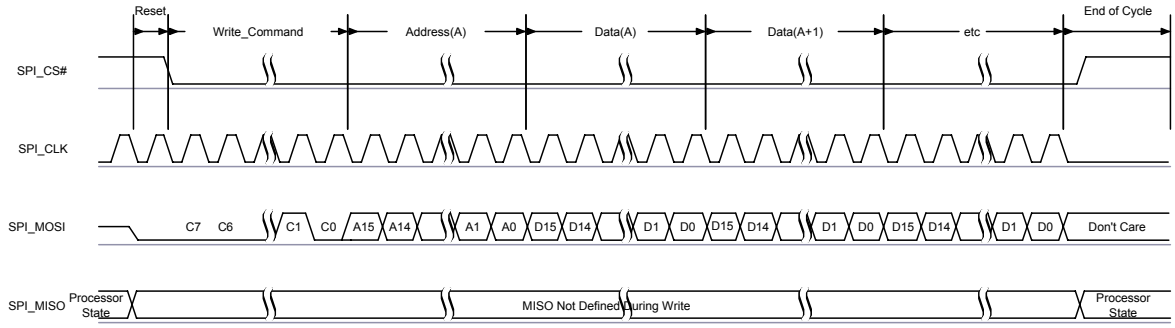


Figure 5.1: SPI Write Operation

5.1.3 Reading from the Device

Reading from BlueCore6-ROM is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore6-ROM then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

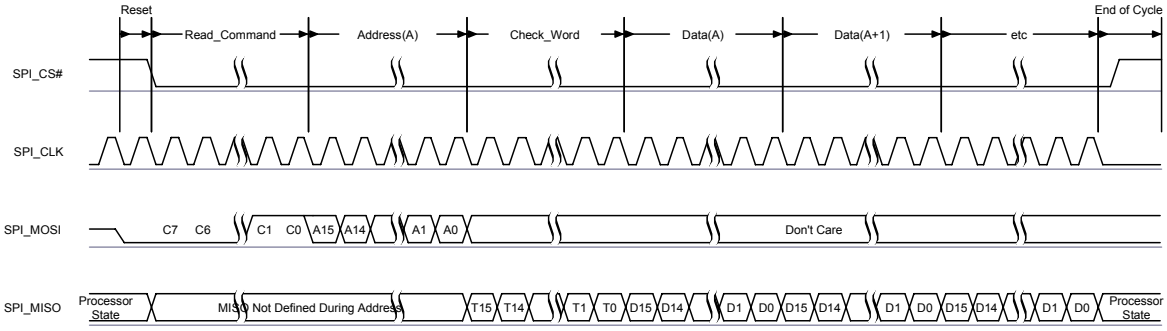


Figure 5.2: SPI Read Operation

5.1.4 Multi-slave Operation

BlueCore6-ROM should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore6-ROM is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore6-ROM outputs 0 if the processor is running or 1 if it is stopped.

6 Host Interfaces

6.1 Host Selection

Pull PIO[4] low to select the UART.

The protocol used by the UART host interface is determined by the status of the UART_MSB and UART_LSB lines at the time PIO[4] is sampled. Table 6.1 lists the different protocols available along with the required configuration of UART_MSB and UART_LSB for each one.

To select a different UART Protocol, connect external 100kΩ pull-up and/or pull-down resistors as appropriate.

For example:

- To select BCSP, connect 100kΩ pull-downs to both UART_MSB and UART_LSB.
- To select H4DS, connect a 100kΩ pull-up to UART_MSB and a 100kΩ pull-down to UART_LSB.

UART_MSB	UART_LSB	UART Protocol
0	0	BCSP
0	1	H4
1	0	H4DS
1	1	H5

Table 6.1: UART Protocol Selection

6.2 UART Interface

This is a standard UART interface for communicating with other serial devices.

BlueCore6-ROM UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

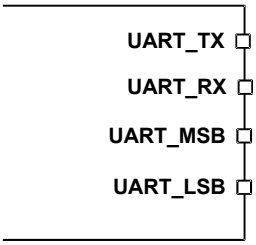


Figure 6.1: Universal Asynchronous Receiver

Two signals implement the UART function, as shown in Figure 6.1. When BlueCore6-ROM is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The signals UART_CTS and UART_RTS are not supported so RS232 hardware flow control cannot be implemented. RS232 software flow control is implemented through BCSP Host Transport.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore6-ROM firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6.2: Possible UART Settings

The UART interface can reset BlueCore6-ROM on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 6.2. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOSTIO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore6-ROM can emit a break character that may be used to wake the host.

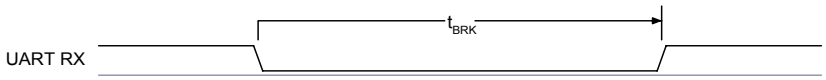


Figure 6.2: Break Signal

Table 6.3 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUDRATE (0x1be). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 6.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 6.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 6.3: Standard Baud Rates

6.2.1 UART Configuration While Reset is Active

The UART interface for BlueCore6-ROM is tri-state while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore6-ROM reset is de-asserted and the firmware begins to run.

7 Audio Interfaces

7.1 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore6-ROM has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore6-ROM offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore6-ROM allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore6-ROM can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz. When configured as a PCM interface slave, it can operate with an input clock up to 2400kHz. BlueCore6-ROM is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting `PSKEY_PCM_CONFIG32` (`0x1b3`).

BlueCore6-ROM interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and µ-law codec
- Motorola MC145481 8-bit A-law and µ-law codec
- Motorola MC145483 13-bit linear codec
- STW 5093 and 5094 14-bit linear codecs
- BlueCore6-ROM is also compatible with the Motorola SSI interface

7.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore6-ROM generates PCM_CLK and PCM_SYNC.

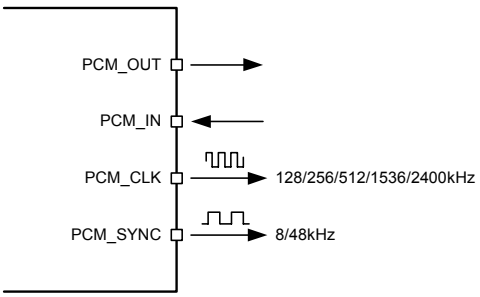


Figure 7.1: PCM Interface Master

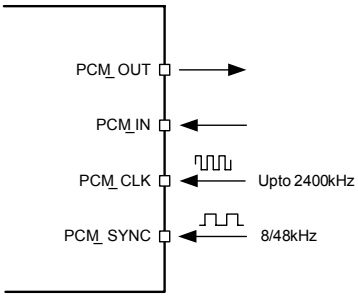


Figure 7.2: PCM Interface Slave

7.1.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore6-ROM is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore6-ROM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

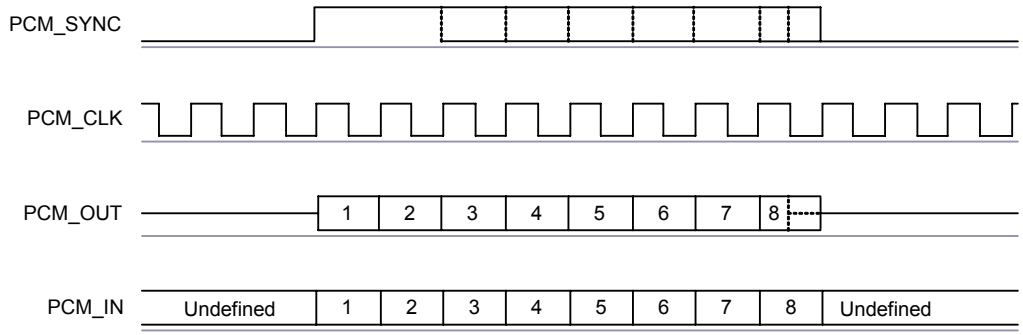


Figure 7.3: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore6-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

7.1.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

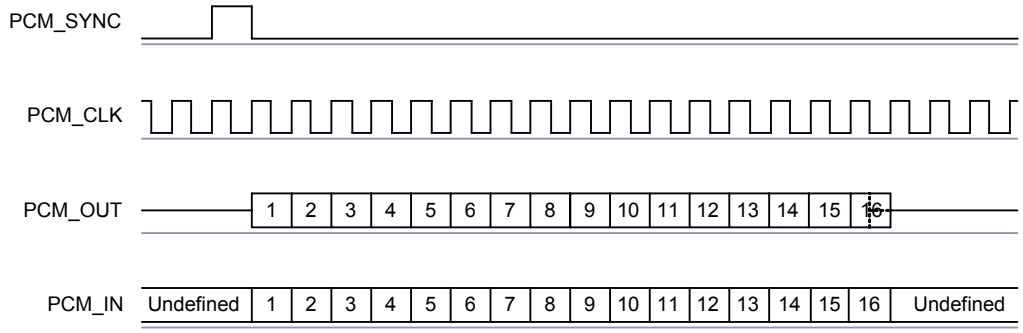


Figure 7.4: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore6-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

7.1.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

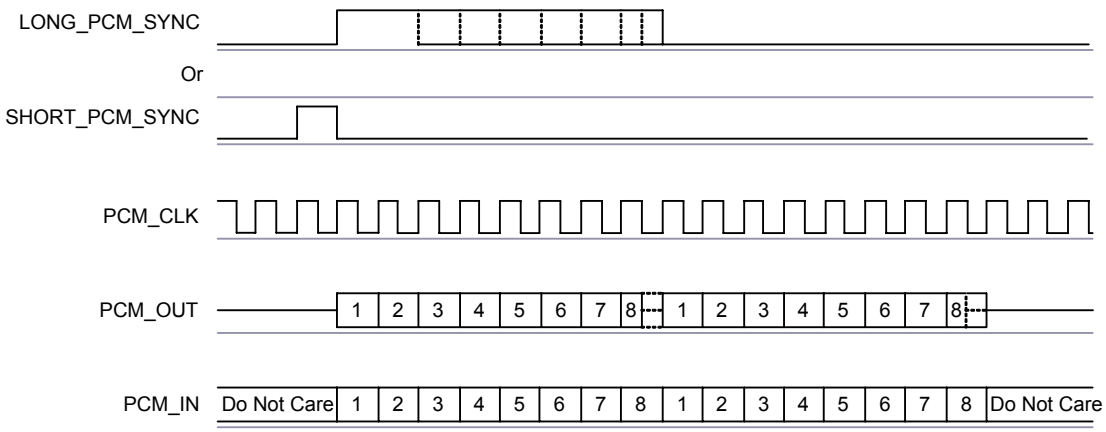


Figure 7.5: Multi-slot Operation with Two Slots and 8-bit Companded Samples

7.1.5 GCI Interface

BlueCore6-ROM is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

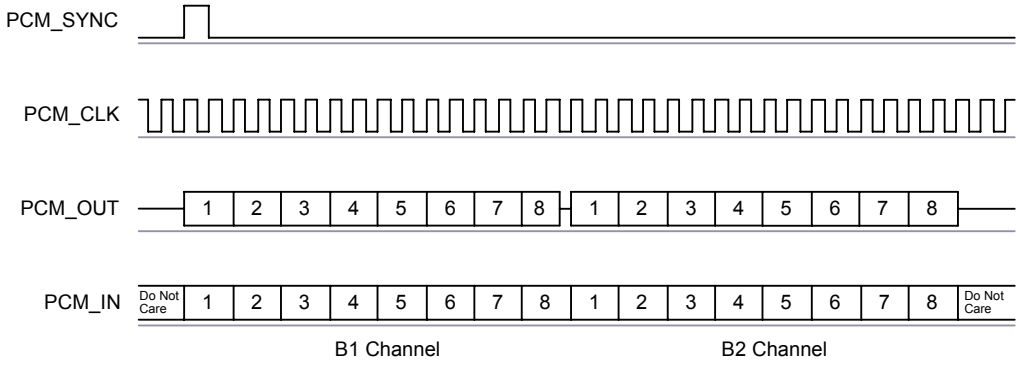


Figure 7.6: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore6-ROM in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz

7.1.6 Slots and Sample Formats

BlueCore6-ROM can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore6-ROM supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola codecs.

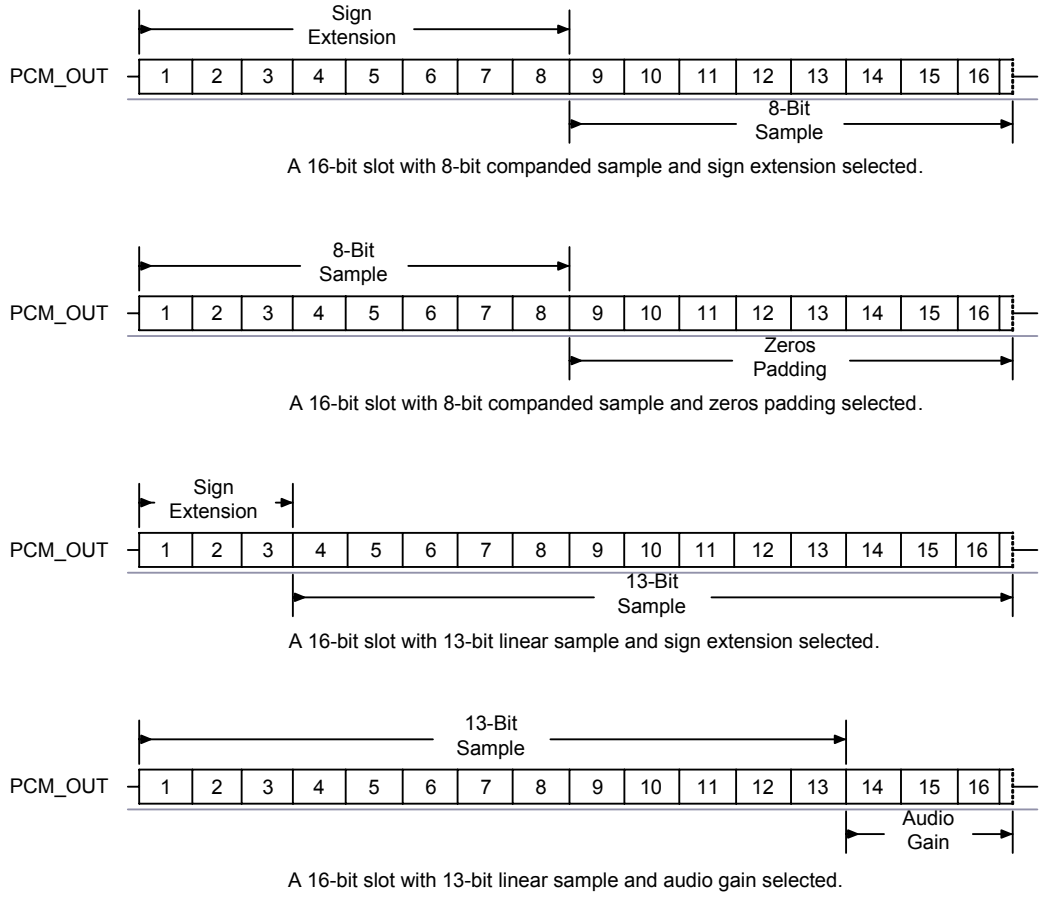


Figure 7.7: 16-Bit Slot Length and Sample Formats

7.1.7 Additional Features

BlueCore6-ROM has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some codecs use to control power down.

7.1.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 7.4.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Table 7.3 and Section 7.1.9.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 7.1: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

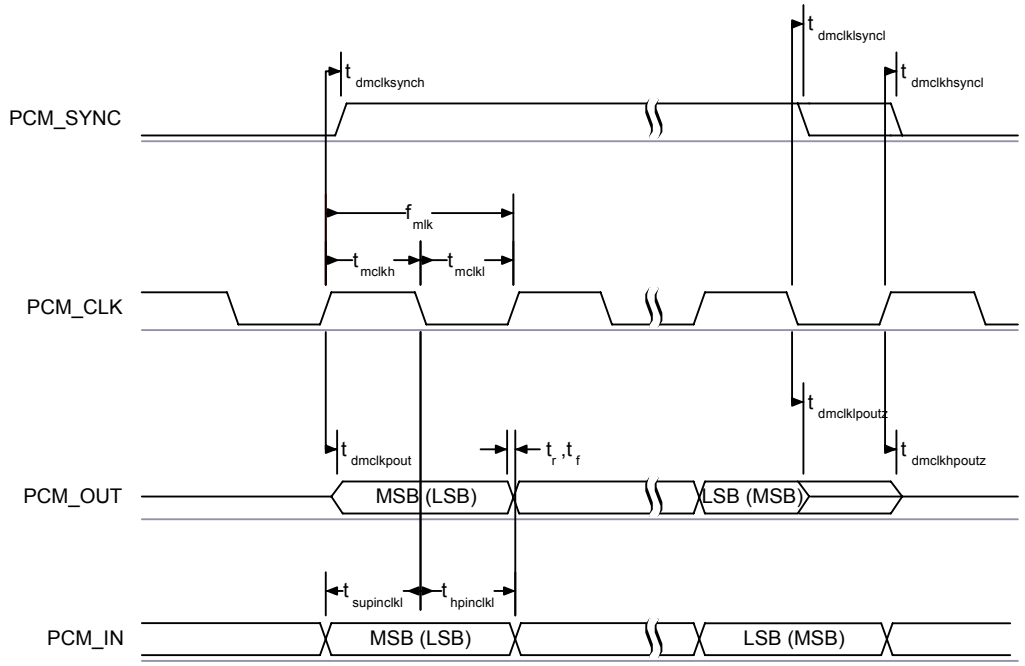


Figure 7.8: PCM Master Timing Long Frame Sync

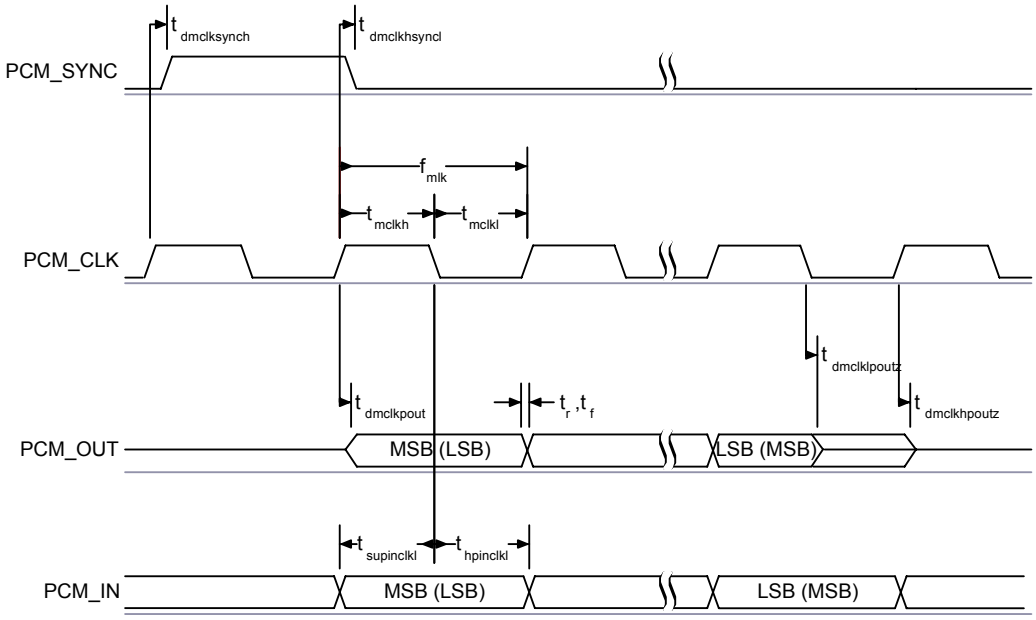


Figure 7.9: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 7.2: PCM Slave Timing

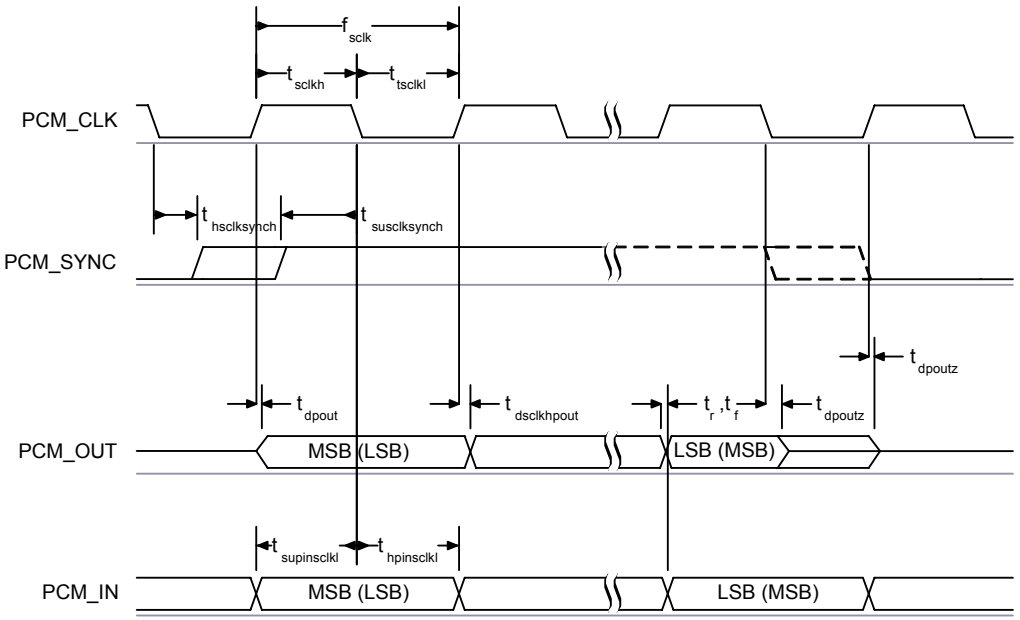


Figure 7.10: PCM Slave Timing Long Frame Sync

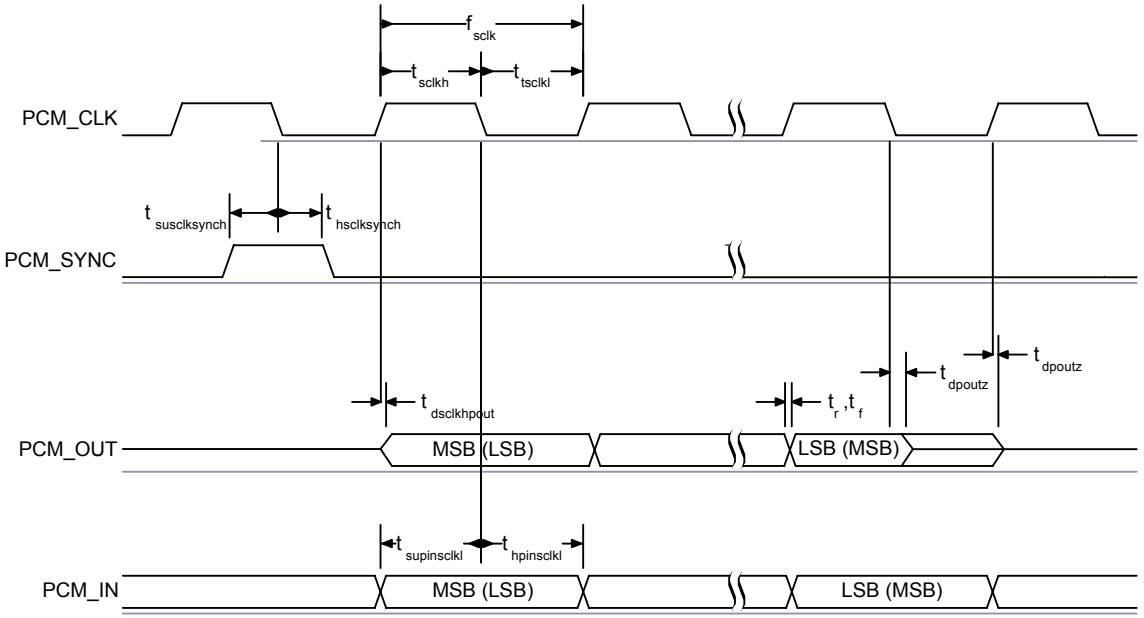


Figure 7.11: PCM Slave Timing Short Frame Sync

7.1.9 PCM_CLK and PCM_SYNC Generation

BlueCore6-ROM has two methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BlueCore6-ROM internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 7.1 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 7.1: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK is set using Equation 7.2 or Equation 7.3 by setting the value of PCM_SYNC_MULT (see Table 7.4) :

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 7.2: PCM_SYNC Frequency Relative to PCM_CLK (PCM_SYNC_MULT = 0)

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT}$$

Equation 7.3: PCM_SYNC Frequency Relative to PCM_CLK (PCM_SYNC_MULT = 1)

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

7.1.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 7.4 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 7.3. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 7.3: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).

Name	Bit Position	Description
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some codecs use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
PCM_SYNC_MULT	12	0 = Sync limit = SYNC_LIMIT x 8. 1 = SYNC_LIMIT.
-	[20:16]	Set to `0b00000`.
MASTER_CLK_RATE	[22:21]	Selects 128 (`0b01`), 256 (`0b00`), 512 (`0b10`) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (`0b00`), 16 (`0b01`), 8 (`0b10`) bit sample with 16-cycle slot duration or 8 (`0b11`) bit sample with 8-cycle slot duration.

Table 7.4: PSKEY_PCM_CONFIG32 Description

7.2 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 7.5 lists these alternative functions. Figure 7.12 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 7.5: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 7.6 describes the values for the PS Key PSKEY_DIGITAL_AUDIO_CONFIG that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_AUDIO_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17-bit SD data is rounded down to 16bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16bit, 01=20bit, 10=24bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17-bit SD_IN data is rounded down to 16bits. For 1 only the most significant 16bits of data are received.

Table 7.6: PSKEY_DIGITAL_AUDIO_CONFIG

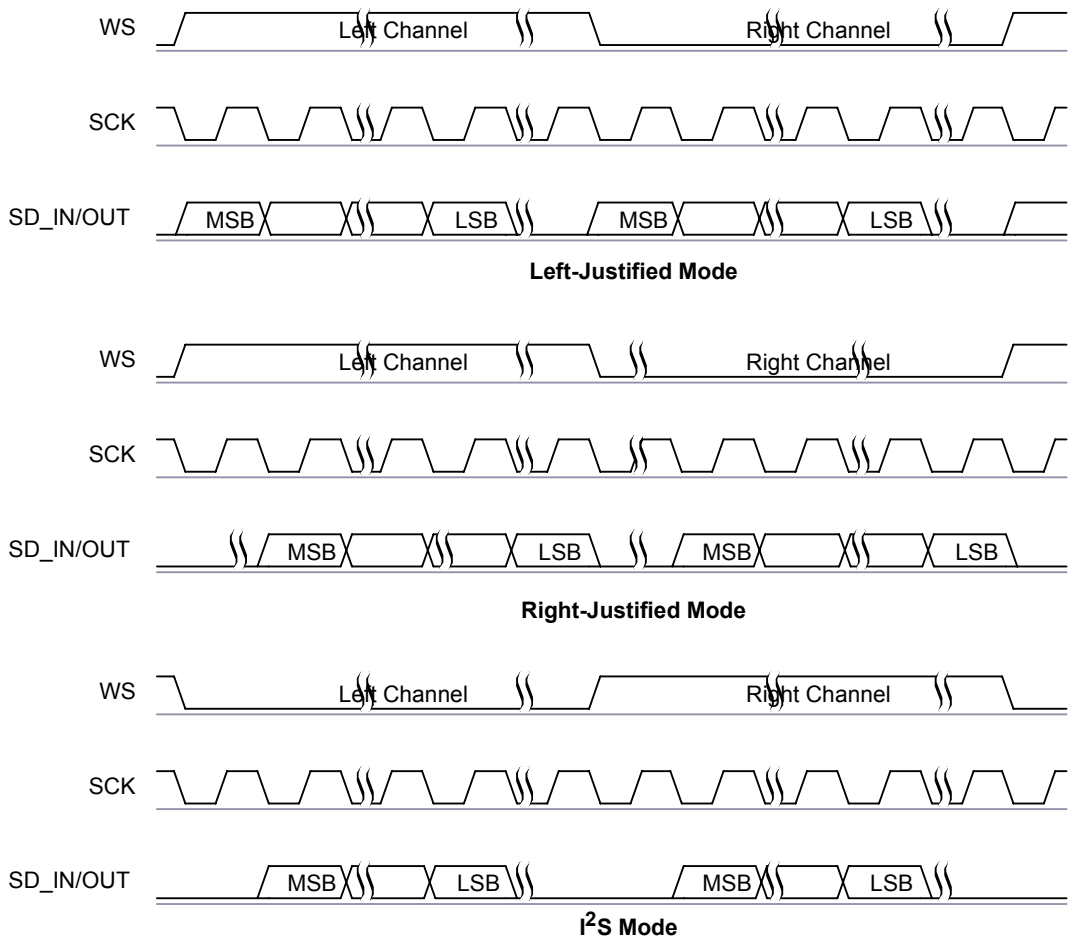


Figure 7.12: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore6-ROM is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 7.7: Digital Audio Interface Slave Timing

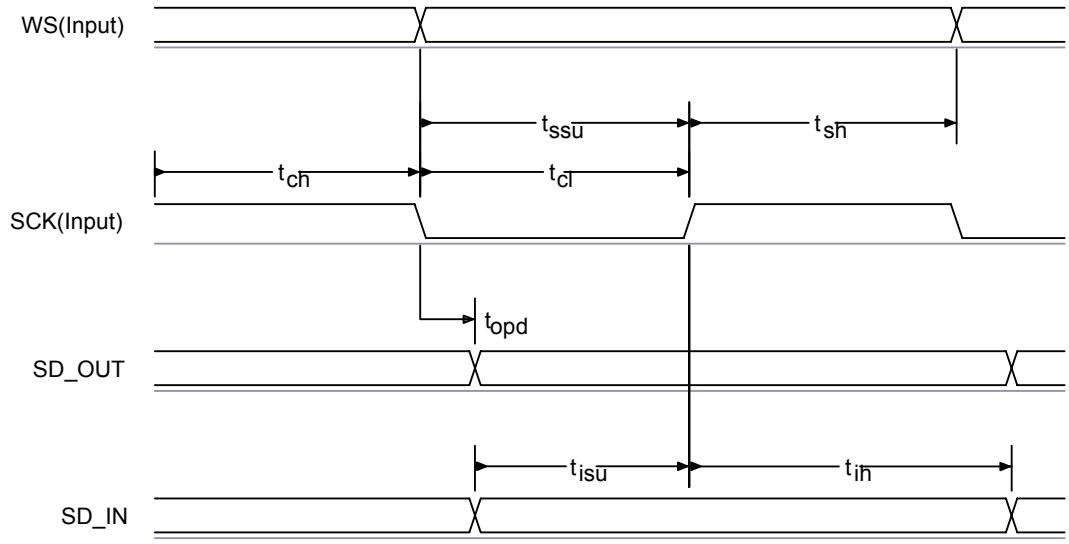


Figure 7.13: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 7.8: Digital Audio Interface Master Timing

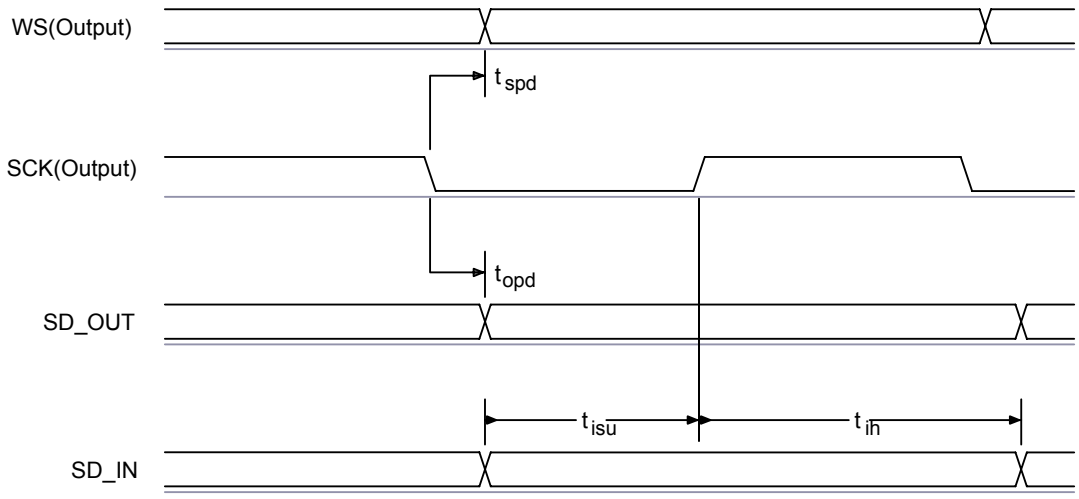


Figure 7.14: Digital Audio Interface Master Timing

8 Power Control and Regulation

BlueCore6-ROM contains a low-voltage regulator to supply the 1.5V core supplies from the 1.8V rail.

The chip can be powered directly from an external 1.8V rail or from an external 1.5V rail omitting the regulator.

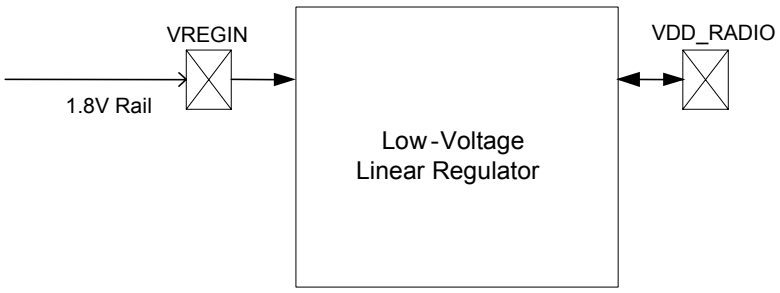


Figure 8.1: Voltage Regulator Configuration

8.1 Sequencing

The 1.5V supplies are VDD_RADIO and VDD_CORE. It is recommended that the 1.5V supplies are all powered at the same time.

The order of powering the 1.5V supplies relative to the other I/O supply (VDD_PADS) is not important. However, if the I/O supply is powered before the 1.5V supplies the digital pads default to their No Core Voltage Reset state. VDD_RADIO should be connected directly to the 1.5V supply; a simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

8.2 External Voltage Source

If the 1.5V rails of BlueCore6-ROM are supplied from an external voltage source, it is recommended that VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels (refer to the average current consumption specification of the regulator).

8.3 Low-Voltage Linear Regulator

The on-chip low-voltage regulator may be used to power all the chip 1.5V supplies. The output of this regulator is connected internally to VDD_RADIO, and must be connected externally to the other 1.5V supply pads. A smoothing circuit using a low ESR capacitor (2.2µF) and a resistor (2.2Ω) to ground should be connected to the output of the regulator. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω. See the Example Application Schematic in Section 9.

This regulator may be enabled by the device firmware.

The regulator is switched into a low power mode when the device is in Deep-Sleep mode, or in reset.

When this regulator is not used the terminal VREGIN must be left unconnected, or tied to VDD_RADIO.

8.4 Reset (RST#)

BlueCore6-ROM may be reset from several sources:

- RST# pin
- Power on reset
- A UART break character
- Via a software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. It is recommended that RST# be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below a threshold. It is released when rising with sufficient hysteresis. See for more information.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown in Table 8.1. Following a reset, BlueCore6-ROM assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore6-ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore6-ROM free runs, again at a safe frequency.

8.4.1 Digital Pin States on Reset

The digital I/O interfaces on the BlueCore6-ROM device are optimised for minimum power consumption after initialisation of digital interfaces.

Table 8.1 shows the pin states of BlueCore6-ROM on reset. `Pull-up` (PU) and `pull-down` (PD) default to weak values unless specified otherwise.

Pin Name/Group	I/O Type	No Core Voltage Reset		Full Chip Reset	
		Pull R	I/O	Pull R	I/O
Reset/Control					
RST#	Digital input	PU	Input	PU	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Digital Interfaces - UART					
UART_LSB	Digital bi-directional	PD	Input	PU	Input
UART_MSB	Digital bi-directional	PD	Input	PU	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
PCM Interface					
PCM_IN	Digital input	PD	Input	PD	Input
PCM_OUT	Digital tri-state output	PD	High impedance	PD	High impedance
PCM_CLK	Digital bi-directional	PD	Input	PD	Input
PCM_SYNC	Digital bi-directional	PD	Input	PD	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
SPI Interface					
SPI_MOSI	Digital input	PD	Input	PD	Input
SPI_CLK	Digital input	PD	Input	PD	Input

Pin Name/Group	I/O Type	No Core Voltage Reset		Full Chip Reset	
		Pull R	I/O	Pull R	I/O
SPI_CS#	Digital input	PU	Input	PU	Input
SPI_MISO	Digital tri-state output	PD	High impedance	PD	High impedance
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
PIOs					
PIO[0]	Digital bi-directional	PD	Input	PD	Input
PIO[1]	Digital bi-directional	PD	Input	PD	Input
PIO[2]	Digital bi-directional	PD	Input	PD	Input
PIO[3]	Digital bi-directional	PD	Input	PD	Input
PIO[4]	Digital bi-directional	PD	Input	PD	Input
PIO[5]	Digital bi-directional	PD	Input	PD	Input
PIO[7]	Digital bi-directional	PD	Input	PD	Input
PIO[9]	Digital bi-directional	PD	Input	PD	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Clocks					
XTAL_IN	Ref clock	None	Input	None	Input
Pin Name/Group	**I/O Type**	**No Core Voltage Reset**		**Full Chip Reset**	
		Pull R	**I/O**	**Pull R**	**I/O**
Test					
TEST_EN	Digital input	Strong PD	Input	Strong PD	Input

Table 8.1: Pin States of BlueCore6-ROM on Reset

9 Example Application Schematic

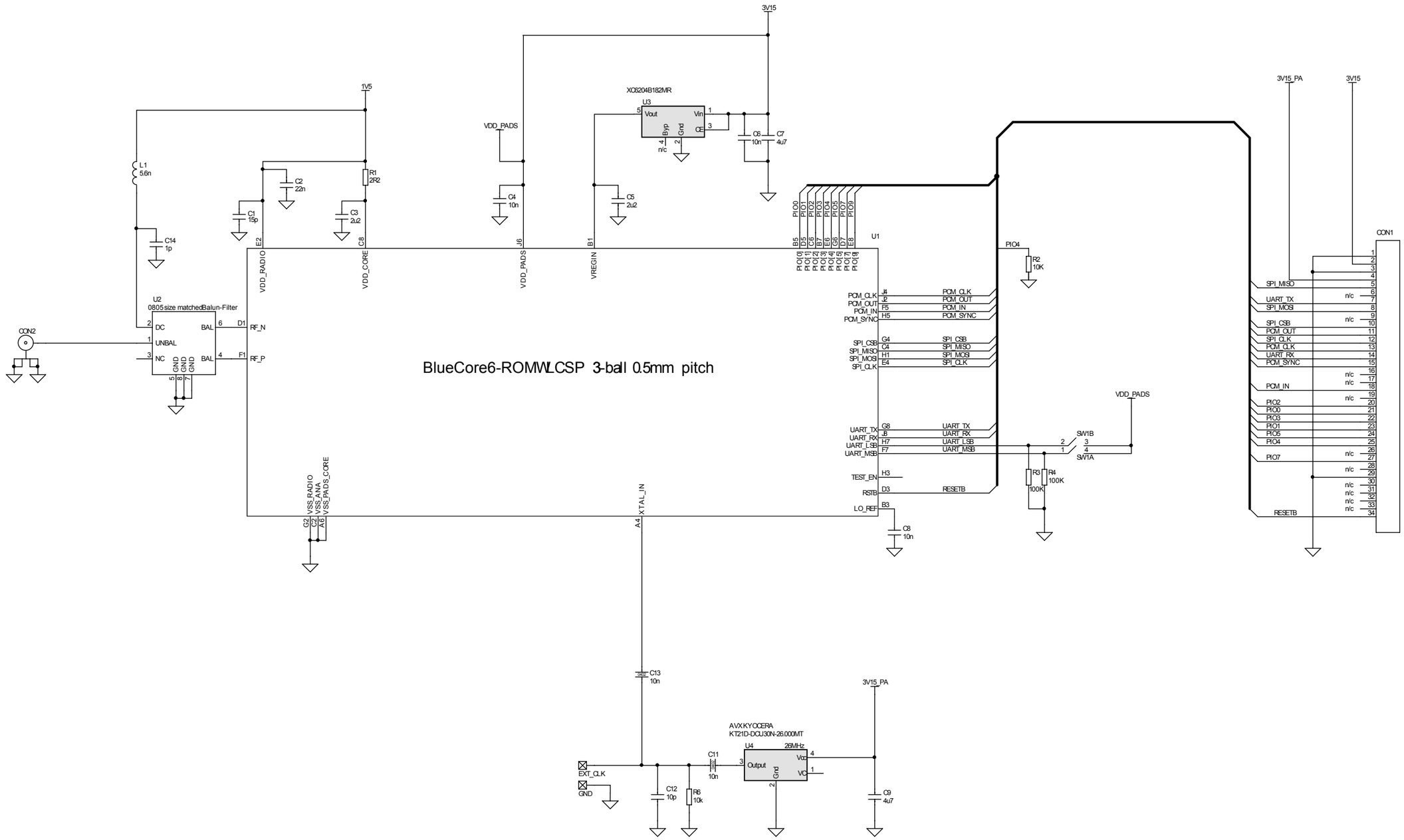


Figure 9.1: Example Application Schematic

10 Electrical Characteristics

10.1 ESD Precautions

BlueCore6-ROM is classified as a JESD22-A114 Class 2 product. Apply ESD static handling precautions during manufacturing.

10.2 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	85	°C
Core Supply Voltage	VDD_RADIO and VDD_CORE	-0.4	1.65	V
IO Voltage	VDD_PADS	-0.4	3.7	V
Supply Voltage	VREGIN	-0.4	2.7	V
Other Terminal Voltages		VSS-0.4	VDD+0.4	V

10.3 Recommended Operating Conditions

Operating Condition		Min	Max	Unit
Operating Temperature Range		-40[a]	85	°C
Core Supply Voltage	VDD_RADIO and VDD_CORE	1.4	1.6	V
IO Voltage	VDD_PADS	1.7	3.7	V

[a] CSR does not guarantee EDR receive sensitivity 8DPSK performance below -30°C.

10.4 Input/Output Terminal Characteristics

Note:

VDD_CORE and VDD_RADIO are at 1.5V unless shown otherwise.

VDD_PADS is at 1.8V unless shown otherwise.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

10.4.1 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.7	-	2.7	V
Output voltage (I_{load} = 70mA / VREGIN = 1.7V)	1.4	1.5	1.6	V
Temperature coefficient	-250	0	250	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (I_{load} < 70mA)	-	-	50	mV/A
Settling time[a] [c]	-	-	50	µs
Maximum output current	70	-	-	mA
Minimum load current	5	-	-	µA
Drop-out voltage (I_{load} = 70mA)	-	-	200	mV
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low Power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	6	10	17	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 70mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode

10.4.2 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low 1.7V ≤ VDD ≤ 3.6V	-0.4	-	+0.25xVDD	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.3	V
Output Voltage Levels				
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 3.6V	-	-	0.125	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 3.6V	VDD-0.4	-	VDD	V
Input and Tri-state Current with:				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	+10	+40	+100	µA
Weak pull-up	-5.0	-1.0	-0.2	µA
Weak pull-down	+0.2	+1.0	+5.0	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input capacitance	1.0	-	5.0	pF

10.4.3 Clocks

Clock Source	Min	Typ	Max	Unit
External Clock				
Input frequency[a]	12	26	52	MHz
Clock input level[b]	0.4	-	VDD_RADIO	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

[a] Clock input can be any frequency between 12MHz to 52MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[b] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_RADIO or above VDD_RADIO. A DC blocking capacitor is required between the signal and XTAL_IN.

10.4.4 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

11 HCI Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval 1.28s	-	0.8	mA
ACL no traffic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1.28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 - hands-free - setting S1	Master	18.5	mA
SCO HV1	Master	37	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	µA
Reset (active low)	-	39	µA

Note:

Conditions: 20°C, VREGIN 1.8V

VDD_PADS: 3.15V

UART BAUD rate: 115.2kbps

Typical Peak Current @ +20°C	
Device Activity/State	**Current (mA)**
Peak current during cold boot	45
Peak TX current Master	45
Peak RX current Master	40
Peak TX current Slave	45
Peak RX current Slave	45
Conditions	
Firmware	HCI 23e
VREGIN	1.8V
Host Interfaces	UART
UART Baud rate	115200
Clock source	26MHz TCXO
RF output power	0dBm

12 CSR Software Stacks

BlueCore6-ROM is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

12.1 BlueCore HCI Stack

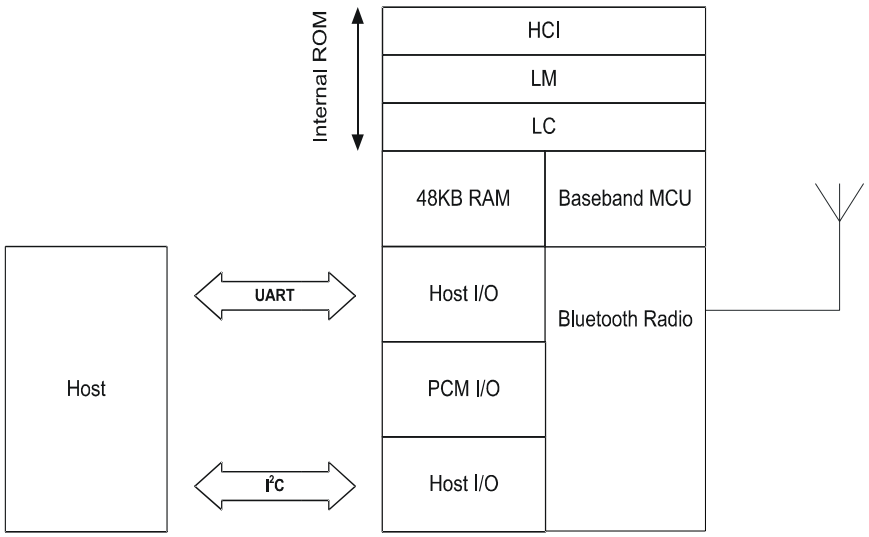


Figure 12.1: BlueCore HCI Stack

In the implementation shown in Section 12.1 the internal processor runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

12.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

CSR supports the following Bluetooth v2.0 + EDR mandatory functionality:

- AFH, including classifier
- Faster connection: enhanced Inquiry Scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- AFH as Master and Automatic Channel Classification
- Fast Connect: Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- eSCO, eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:
  - Baseband, including LC
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps . This is the maximum allowed by Bluetooth v2.0 + EDR specification
- Operation with up to 7 active slaves
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7. BlueCore6-ROM Supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification
- Maximum number of simultaneous active SCO connections: 3
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page Scan and Inquiry Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

12.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BCSP, a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting deep sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD, provides:
  - Access to the IC's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the IC's external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the IC's PS configuration database. The database sets the device's Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, constants, etc.
- A UART break condition can be used in three ways:
  6.1 Presenting a UART break condition to the IC can force the IC to perform a hardware reboot
  6.2 Presenting a break condition at boot time can hold the IC in a low power state, preventing normal initialisation while the condition exists
  6.3 With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a deep sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the IC's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: shallow sleep and deep sleep. The IC drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the IC's PCM ports (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the firmware release note for the specific functionality of a particular build.

12.2 BCHS Software

BCHS is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies), SPI
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

12.3 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore6-ROM hardware and software, and as toolkits for developing on-chip and host software.

13 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART	33-ball WLCSP (Pb free)	3.21 x 3.49 x 0.6mm (max.), 0.5mm pitch	Tape and reel	BC6888A04-ICXL-R

Note:

Minimum Order Quantity

2kpcs taped and reeled

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

13.1 Tape and Reel Information

For tape and reel packing and labeling see *IC Packing and Labelling Specification*.

13.1.1 Tape Orientation

The general orientation of the WLCSP in the tape is as shown in Figure 13.1.

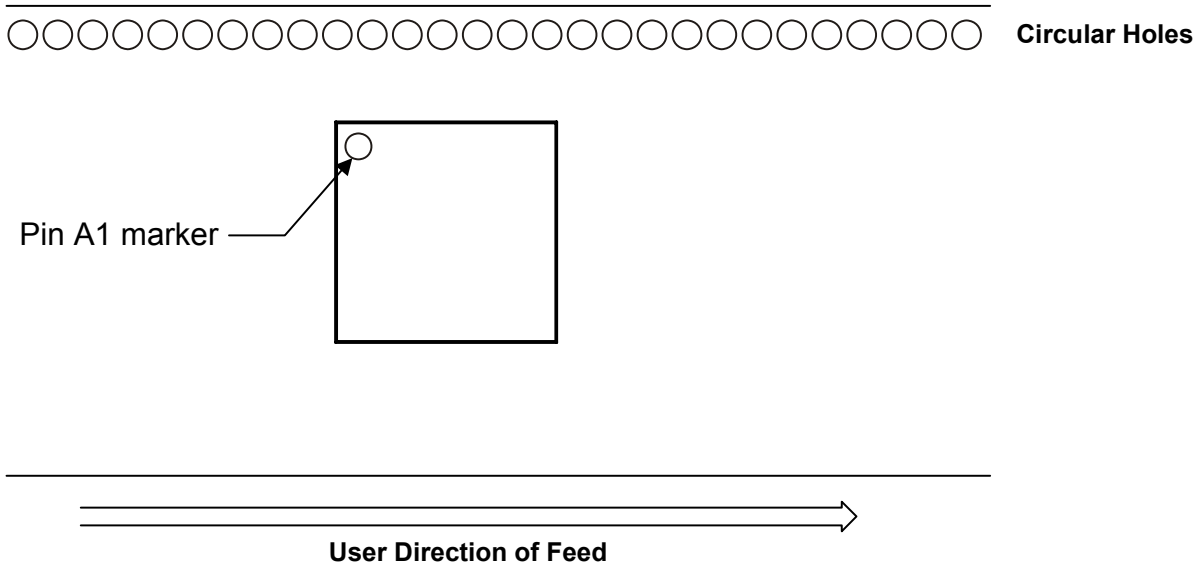
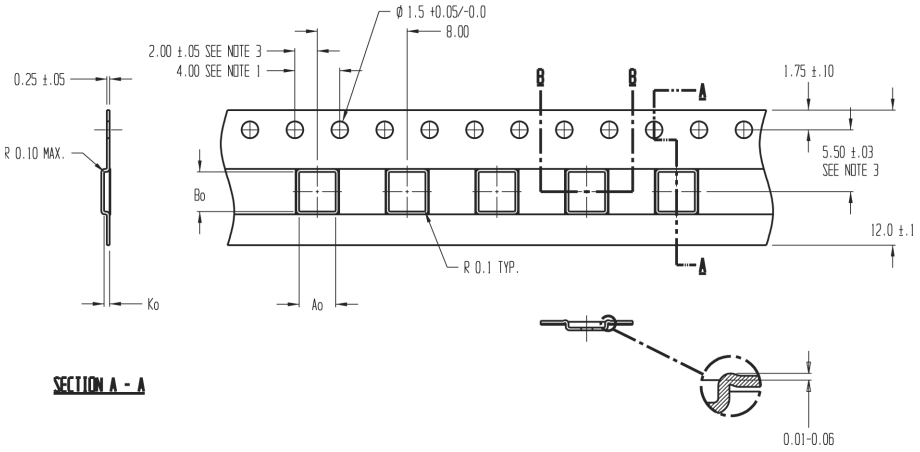


Figure 13.1: Tape and Reel Orientation

13.1.2 Tape Dimensions



A_0	B_0	K_0	Unit	Notes
3.31	3.65	0.92	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.02 2. Camber in compliance with EIA 763 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

13.1.3 Reel Information

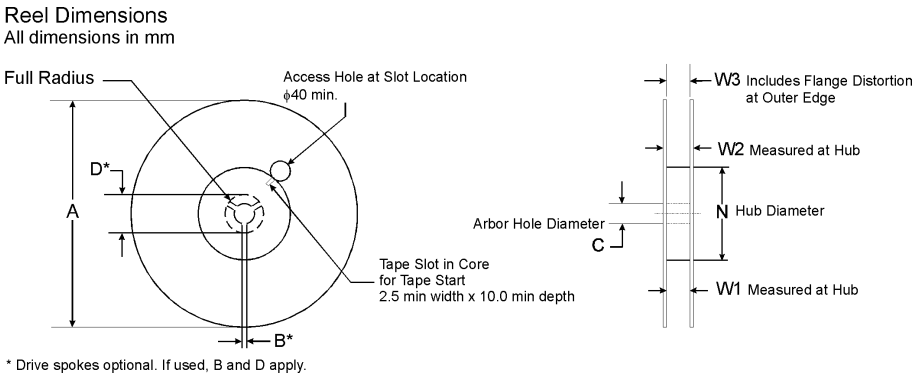


Figure 13.2: Reel Dimensions

Package Type	Tape Width	A Max	B	C	D Min	N Min	W1	W2 Max	W3		Units
									Min	Max	
3.21 x 3.49 x 0.6mm WLCSP	12	330	1.5	13.0 (+0.5/-0.2)	20.2	50	12.4 (+2.0/-0.0)	18.4	11.9	15.4	mm

Table 13.1: Reel Dimensions

14 Document References

Document:	Reference, Date:
BCCMD Commands	CS-101482-SPP (bcore-sp-005P)
Core Specification of the Bluetooth System	v2.1 + EDR, 31 July 2007
Core Specification of the Bluetooth System	v2.0 + EDR, 10 November 2004
CSR Bluetooth Coexistence Implementations	CS-110632-AN
HQ Commands	CS-101677-SPP (bcore-sp-003P)
IC Packing and Labelling Specification	CS-112584-SPP

Terms and Definitions

Term	Definition
802.11™	WLAN specification defined by a working group within the IEEE
ADC	Analogue to Digital Converter
ADPCM	Adaptive Differential Pulse Code Modulation (e.g G.726)
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AuriStream	CSR proprietary ADPCM codec
BCCMD	BlueCore Command
BCHS	BlueCore Host Software
BCSP	BlueCore Serial Protocol
BIST	Built-In Self Test
BMC	Burst Mode Controller
codec	Coder decoder
CSR	Cambridge Silicon Radio
CVSD	Continuous Variable Slope Delta Modulation
DDS	Direct Digital Synthesis
EDR	Enhanced Data Rate
eSCO	Extended SCO
ESD	Electro-Static Discharge
FSK	Frequency Shift Keying
GCI	General Circuit Interface
GSM	Global System for Mobile communications
H4DS	H4 Deep Sleep
HCI	Host Controller Interface
IQ	In-Phase and Quadrature
I/O	Input/Output
I^2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
IF	Intermediate Frequency
L2CAP	Logical Link Control and Adaptation Protocol
LC	An inductor (L) and capacitor (C) network
LM	Link Manager
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
Mbps	Megabits per second
MCU	Micro Controller Unit
MSB	Most Significant Bit (or Byte)
NSMD	Non Solder Mask Defined
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant

Term	Definition
PIO	Programmable Input Output
PND	Personal Navigation Device
PS	Persistent Store
PS Key	Persistent Store Key
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP; element of Bluetooth
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RSSI	Received Signal Strength Indication
SCO	Synchronous Connection-Oriented
SDP	Service Discovery Protocol; element of Bluetooth
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access
WCS	Wireless Co-existence System
WLCSP	Wafer Level Chip Scale Package