TELEGENT SYSTEMS

TLG1100

Ultra-Low Power NTSC/PAL TV-On-Chip

Description

The TLG1100 is a high performance, ultra-low power RF tuner combined with an NTSC/PAL compatible video decoder on a single chip. The TLG1100 is a true single-chip design, requiring no external SAW or ceramic filters to achieve full channel selectivity with an average power consumption is only 250 mW. Capable of receiving any channel from 50 to 800 MHz, designs employing the TLG1100 can be deployed for analog television reception nearly worldwide with only minimal software changes.

The TLG1100 utilizes a direct-conversion, zero-IF architecture that allows for extremely good image and adjacent channel signal rejection. A wideband, low-noise amplifier is used to receive the entire video signal band from the antenna, and provides a gain range in excess of 60 dB. A single down conversion I/Q mixer then translates the desired channel to DC.

At baseband, an anti-aliasing filter is combined with a second 60 dB variable-gain amplifier to provide the first level of adjacent-channel rejection, as well as provide signal conditioning for interfacing into the dual 10-bit analog-to-digital converters. Subsequent processing by the DSP provides final adjacent-channel rejection and audio/video carrier demodulation. The audio stream is FM-demodulated and passed to the audio output port, whereas the CVBS video stream is separated into component video and output onto the video data bus.

Telegent Systems' SureTrak™ DSP-based tuner architecture enables several unique features in the decoder that make it ideal for the mobile reception environment. Unlike conventional analog decoders, the TLG1100 can compensate for multi-path fading thereby preventing severe ghosting and picture degradation when the receiving antenna is small and in-motion. In addition, if momentary signal dropout is detected, the TLG1100 can be programmed to hold the prior frame, preventing severe breakup in the perceived image. For high-speed motion applications, the SureTrak™ architecture provides automatic Doppler compensation for time-varying frequency shifts as high as 50 Hz.

The output of the video decoder is an 8-bit parallel component video stream interface compliant with CCIR/ITU 601; video timing is entirely generated internally. Also, an adaptive 2D comb filter is available for enhanced color fidelity on larger displays. Both analog and digital audio (I2S) is supported. All configuration control and register access is done via a 2-wire (I2C-compliant) serial port.

As an additional feature, the TLG1100 directly supports worldwide FM radio reception without requiring any additional components.

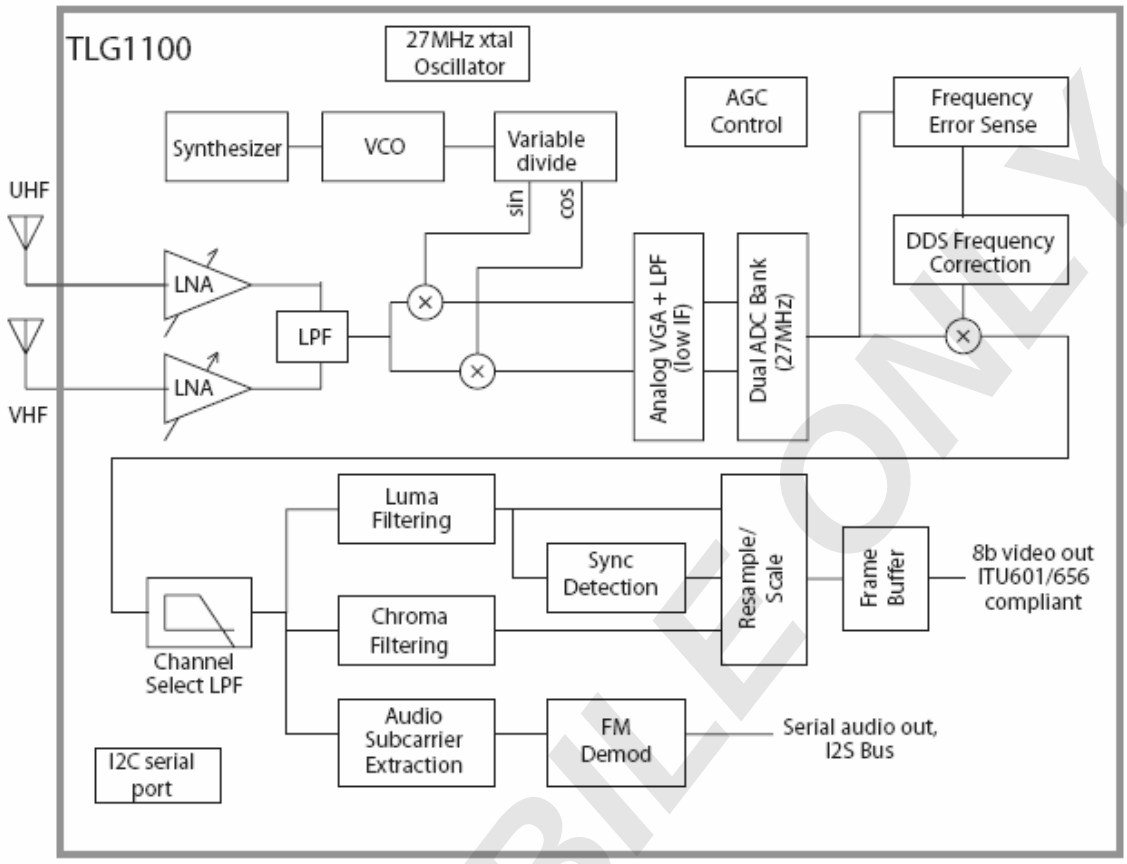
Features

- Fully integrated, single-chip tuner plus NTSC/PAL decoder
- Worldwide FM radio reception
- 250 mW power consumption
- Zero-IF down conversion architecture
- SureTrak™ digital signal processing
- Minimal external passive components
- 48-800 MHz RF reception
- 100 dB dynamic range
- <6 dB noise figure
- Fully integrated digital AGC loop
- Fully integrated channel selectivity
- 35 dBc first-adjacent rejection
- Internal blank-level clamping
- Dynamic ghosting/fading compensation
- Clocked from a single 27 MHz crystal
- All-digital video timing generation
- CCIR/ITU-601 compliant 8-bit parallel video output
- Analog and I2S digital audio output
- I2C-compliant two-wire control port
- 2.8V RF supply, 1.2V digital supply
- 68-pin MLF/QFN package

Applications

- Cellular phone television reception
- Personal video players
- Car-mounted televisions
- Adapter/PCMCIA multimedia tuners
- Personal digital assistants
- Laptop computers

Architecture



Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device under conditions other than those listed in the Electrical Parameters section is not recommended or implied. Exposure to any of the absolute-maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	MIN	MAX	UNIT
Supply voltage		6	V
Junction temperature[1]		130	°C
Operating temperature	-10	85	°C
Storage temperature	-40	150	°C
Lead solder temperature for 4 seconds		245	°C
Relative humidity		95	%
Input voltage	-0.3	Vdd +0.3	V

Electrical Parameter Specifications

PARAMETER	MIN	TYP	MAX	UNIT	Notes
General					
Power consumption		250		mW	Time average
Input frequency range	48		800	MHz	
Supply voltage, Analog + I/O	2.7	2.8	2.9	V	
2.8V current consumption					
Active		75		mA	
Standby			1.5	mA	
Shutdown			50	uA	Supply still applied
Supply voltage, Digital core	1.14	1.2	1.26	V	+/- 5%
1.2V current consumption					
Active		35		mA	
Standby			100	uA	
Shutdown			100	uA	Supply still applied
Wakeup time from standby			10	msec	
Wakeup time from shutdown			50	msec	Time from shutdown to start of VSync lock detect (ADC output valid)
Operating temperature	-10		85	°C	
Clock frequency		27		MHz	
Crystal accuracy			50	Ppm	Relative to 27 MHz
RF Down Conversion Path					
RF LNA gain range	55	60		dB	Digital PGA
RF LNA maximum gain		35		dB	Voltage gain
RF gain step size		2		dB	6b digital gain control
Noise figure		5	6	dB	
CTB			45	dBc	
Video sensitivity		-75		dBm	With recommended reference design
CSO			50	dBc	
OIP3	67			dBmV	Output referred @ baseband filter
1dB Compression		57		dBmV	Output referred @ baseband filter
2^{nd} Adjacent Rejection		20		dBc	Analog interferer
VSWR			2:1		Relative to 50 ohms
RF gain flatness		6		dB	48-800 MHz
Channel flatness			3	dB	Across 8 MHz
Image rejection	45			dBc	
Oscillator Section					
Tuning range	2.0		3.5	GHz	Minimum div-4 for actual mixer LO signal
Phase Noise @					
10 kHz		85		dBc	
100 kHz		103		dBc	

1 MHz		130		dBc	
Spurious			-50	dBc	
LO Stepsize			62.5	KHz	
VCO compliance range		1.5		V	
Frequency lock time			2	msec	
LO leakage		-80		dBm	Measured at RFIN port
Baseband/ADC Section					
Antialias filter	2.5		4	MHz	Active RC, calibrated
Antialias filter stepsize		0.5		MHz	
Antialias cutoff accuracy	-5		+5	%	Percent of target, Post calibration
PGA Maximum Gain		50		dB	Voltage gain
PGA Gain Range		60		dB	
PGA Gain Stepsize		0.5		dB	
PGA distortion		70		dBc	Output referred; two-tone test @ 1 MHz
ADC input voltage swing		1		V	Peak-peak differential
ADC resolution		10		bits	
ADC DNL			0.5	LSB	
ADC INL			1	LSB	Post calibration
ADC Clock Frequency		27		MHz	Synchronous with PLL pre-scalar
RF AGC loop bandwidth			1	kHz	
Video DSP Demodulator/Decoder Section					
Video IF carrier	1		3	MHz	Digital direct synthesis
Video IF carrier stepsize			62.5	kHz	
Frequency tracking loop bandwidth			200	kHz	
Doppler correction			50	Hz	
Differential phase		0.5	1	Degree	
Differential gain			0.1	dB	Post-calibration and equalization
Luma nonlinearity			1	%	
Luma brightness error			1	%	
Luma contrast error			1	%	
Hue phase error			0.5	Degree	
Color gain adjust	0		12	dB	Digital gain control
Chroma amplitude error		0.2		%	
Color saturation error			1	%	
Horizontal lock time		60		lines	
Vertical lock time		2		VSyncs	
Ghosting equalizer lock time		200		lines	
Loss-of-signal detection	50			HSync	Min. time before signal loss asserted

Functional Description

RF Down Conversion Block

The RF down conversion block comprises a highly linear, high dynamic range LNA coupled with a true zero-IF mixer plus baseband signal processing. Internally, the LNA and mixer have an overall gain range in excess of 60 dB, giving the TLG1100 excellent performance under mobile conditions. The mixer plus baseband signal processing are implemented using a proprietary architecture, which eliminates the need for any external SAW filters while maintaining dynamic range within the receiver. At baseband, an anti-aliasing filter is combined with a second 60 dB variable-gain amplifier to provide the first level of adjacent-channel rejection, as well as provide signal conditioning for interfacing into the analog-to-digital converters. A pair of on-chip, high-performance analog-to-digital converters bridge the RF down conversion block with the digital signal processing for the demodulator and decode functions.

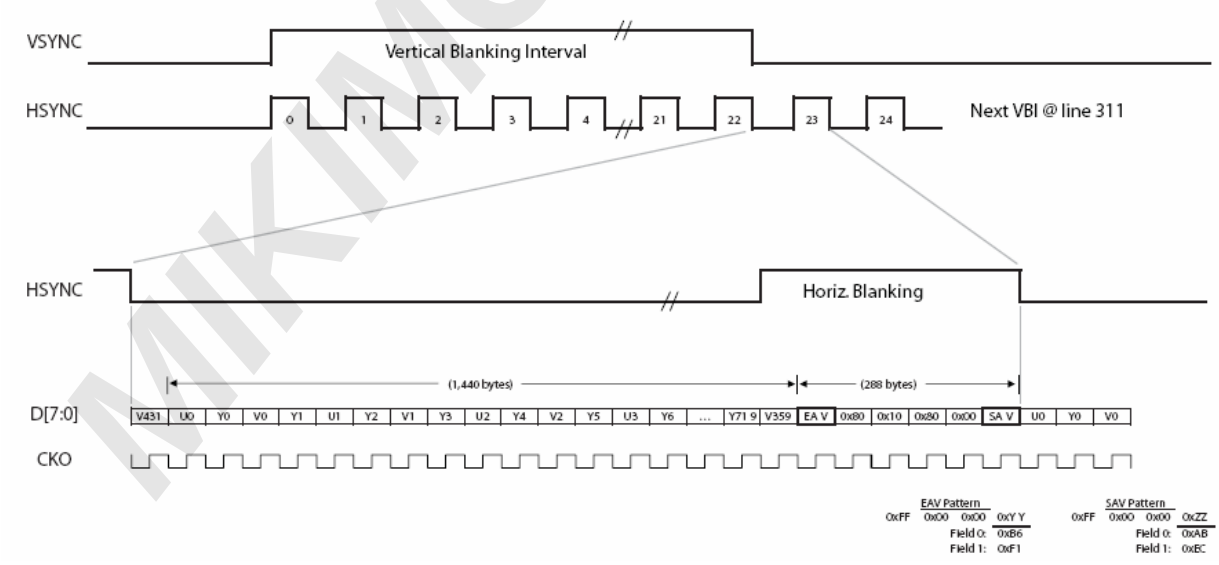
NTSC/PAL Demodulator and Decoder

The Demodulator receives the digitized I/Q signals from the Analog-to-Digital converters. Digital offset and gain control blocks condition the signals for the rest of the signal processing. Channel-select filtering in the digital domain is applied to further reduce nearby adjacent channel interferers and improve signal isolation. The data is then separated into 3 streams of Luma, Chroma, and Audio. The Audio stream is FM-demodulated according to the register-selected audio standard. The Luma and Chroma data streams are decoded to form 601-compliant fields, with framing information derived in a Sync Detection block. The Sync Detection block extracts VSync and HSync timing information from the demodulated data stream in a robust fashion, and is able to indicate when signal quality is low. This quality information can be used to control a frame-hold buffer to maintain an image through momentary dropouts, thereby improving the perceived quality of the video output. The following video signal standards are supported in the Demodulator/Decoder block: NTSC-M, PAL-D, K, B, G, H, and I. Specific audio support is documented further below.

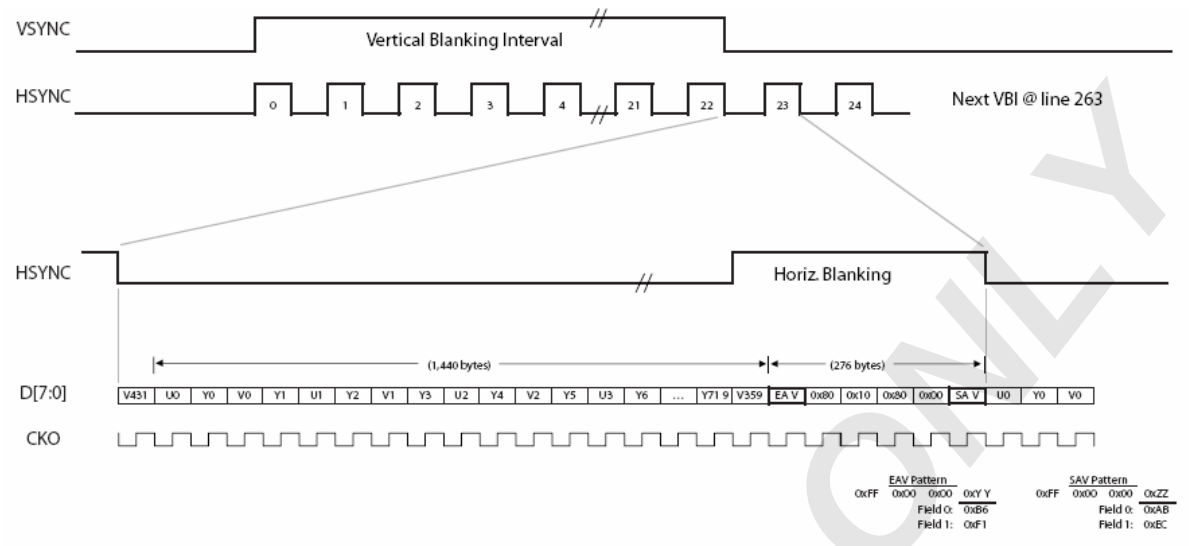
ITU-601 Interface

The digital video output port consists of an ITU-601 compliant 8-bit 4:2:2 (YCbCr) parallel interface. Additional hardware hsync and vsync lines are provided for maximum flexibility in interfacing with existing designs. The timing for the bus is as follows:

625 Timing

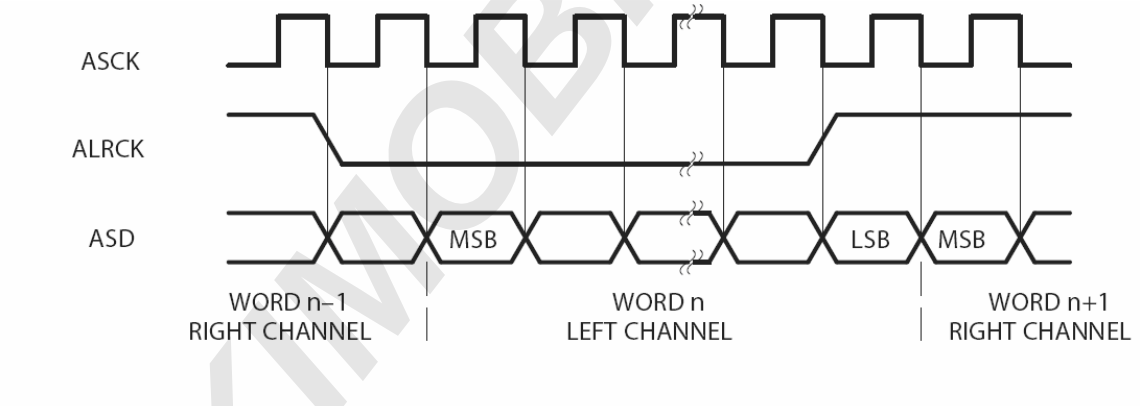


525 Timing



Audio Interface

Audio output on the TLG1100 can be either in digital (mode 1) or analog (mode 2) form. In mode 1, the four signals on the audio port represent an I2S-compliant signal either running in slave mode (ASCK as the clock input) or master mode (AMCK as the master clock output). The ALRCK signal is the word select line for left/right audio samples. The timing on the bus is as follows:



Note that in master mode, the available clock output frequencies are 48.0427 kHz or 31.991 kHz, both of which are integer submultiples of the master 27 MHz crystal clock frequency. This is a requirement, owing to RF noise mitigation concerns.

In slave mode the receiving device supplies the desired audio frequency. Output bit resolutions of 16, 20 and 24 bits are supported, but the actual number of significant bits will be 16.

In mode 2, the left/right audio signals are output as 1-bit sigma-delta modulated waveforms on two pins (single-ended output, one pin each for left- and right- audio channels). The output impedance is designed to drive into a load impedance > 10k ohms, and the sigma-delta reconstruction filter needs to be

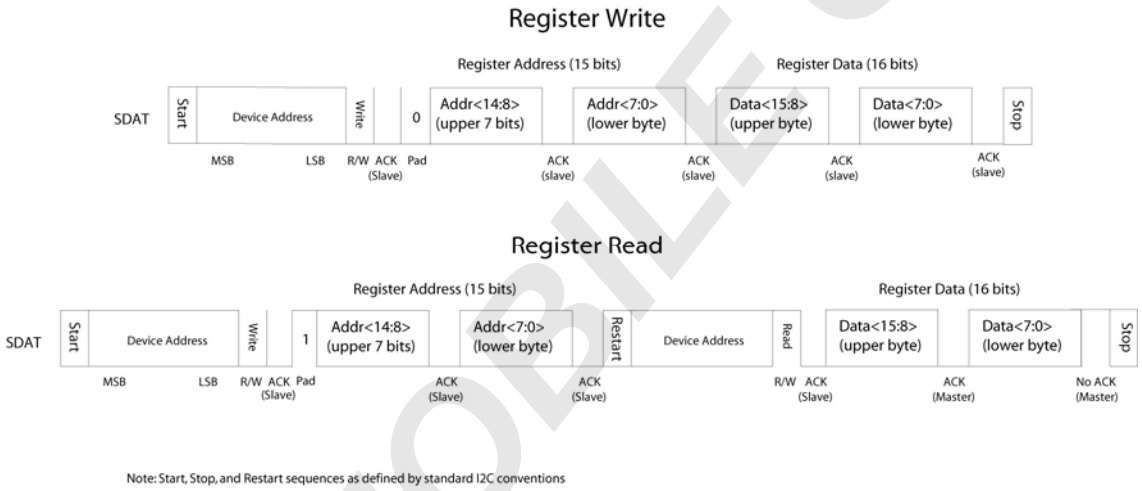
implemented on the board. For use in mode 2, the recommended board design for the reconstruction filter is a 3rd order LRC lowpass. For details, please refer to the TLG1100 reference design.

Note that the TLG1100 only supports monaural analog FM audio; the same sample is duplicated in both L/R channels for mode 1, and the same signal is currently fed out through both analog output pins in mode 2. Currently, there is no SAP support in the TLG1100.

A Left-justified mode is also supported when running in slave mode, in addition to the standard I2S data alignment. In this mode the MSB is output on the first clock following a change in ALRCK.

Serial Control

The TLG1100 features a two-wire serial port for setting internal registers on the chip. Signaling on these two lines is compliant with I2C, and the TLG1100 is a slave-only device. Maximum clock speed on the line is 400 KHz, and the device will only respond to its unique address, allowing it to share the bus with other devices utilizing the same signaling standard. However, since this is a high-performance RF device, care must be taken to minimize switching noise on any digital input to the chip. In particular, if multiple devices share the serial control bus, the control lines should not route anywhere nearby the RF LNA input lines and proper shielding measures done as part of the board design. The timing diagrams for read/write are as follows:



Note: Start, Stop, and Restart sequences as defined by standard I2C conventions

Since both address and data for the TLG1100 are wider than 8 bits, upper and lower bytes are written consecutively as shown. In particular, note that the address is 15 bits wide, with the upper 7 bits padded with either a 1 or a 0 to complete the upper byte. The upper address byte must be padded by a “0” in the case of a write, and padded by a “1” in case of a read. The Start, Stop, and Restart sequences as indicated in the diagram are compliant with I2C conventions.

There is no provision for command restart within the device (a register read/write must complete; otherwise, the device ignores the partial read/write). Likewise, there is no provision for auto-incrementing for consecutive writes to sequential addresses. The 7-bit device address for the TLG1100 is 0x2c (but in the case of a conflict with another device on the same I2C bus, setting GPIO4 will change the address to 0x2d).

Frequency Synthesis and Master Timing

The TLG1100 takes a single external 27 MHz crystal as its master timing reference; this reference is used as both the ADC time base as well as the basis for the overall frequency synthesis loop. Although it is

possible to use an external 27 MHz clock source instead of the crystal, the jitter and phase noise performance needed for precision RF tuning makes use of an external source difficult unless frequency accuracy can be guaranteed.

Programming the channel carrier frequency for the TLG1100 involves two register writes, which must be done in this sequence. Four values are needed to determine the channel carrier frequency, and the LO carrier frequency must be set to the *center* frequency of the desired channel (in particular, it should *not* be set to the video carrier frequency). The LO carrier frequency is given by the following equation:

LO frequency = (Xtal frequency / synth_r_cnt) * (32* synth_bcnt + synth_acnt) / (synth_lo_div)

The driver software should have a lookup table that associates channel number (e.g., channel 19) with 6 values:

(synth_r_cnt<7:0>, synth_lo_div<2:0>, synth_bcnt <8:0>, synth_acnt<4:0>,
cp_bias<1:0>, filt2_cal_seed<9:0>)

The nominal value for the R count (synth_r_cnt) should be 108, corresponding to a PLL update rate of 250 kHz. The R count, LO_div, Bcnt, and Acnt are used by the synthesizer to determine the LO frequency; cp_bias and filt2_cal_seed are frequency-dependent parameters that are needed for the calibration routines (see below).

The TLG1100's time-to-frequency-lock is less than 2 milliseconds.

Calibration and Sequencing

The TLG1100 has several unique DSP-based calibration routines that enhance mixed-signal performance without incurring additional power consumption. The calibration routines are started by a write to a particular register specific to that calibration (i.e., a write to the "ADC_CAL" register would start the converter calibration), and completion status is indicated by a bit within the master calibration status register. The three master calibrations are:

- Converter calibration
- Filter cal I
- Filter cal II

Filter cal II has a channel-dependent value (the seed), which must be stored in software as part of the channel assignment table along with the R count, Acnt, Bcnt, and cp_bias values for the synthesizer (as described above).

Power-up

On power up of the device from a cold condition, the chip must be put into a known state. The sequence of operations is:

1. Power-on reset (active low) must be asserted for 1 millisecond
2. Activate converter calibration by a write to the ADC_CAL register
3. Upon completion of converter calibration (checked by polling the master calibration status register), activate filter cal I
4. Upon completion of filter cal I, set the channel carrier frequency by programming the synthesizer to the desired value (as documented above)
5. Upon frequency lock detect (again indicated by the frequency lock detect bit in the master calibration register), write the associated channel seed (filt2_cal_seed<9:0> into the FILT2_CAL register for filter cal II. This activates the final calibration for filter cal II.

Channel change

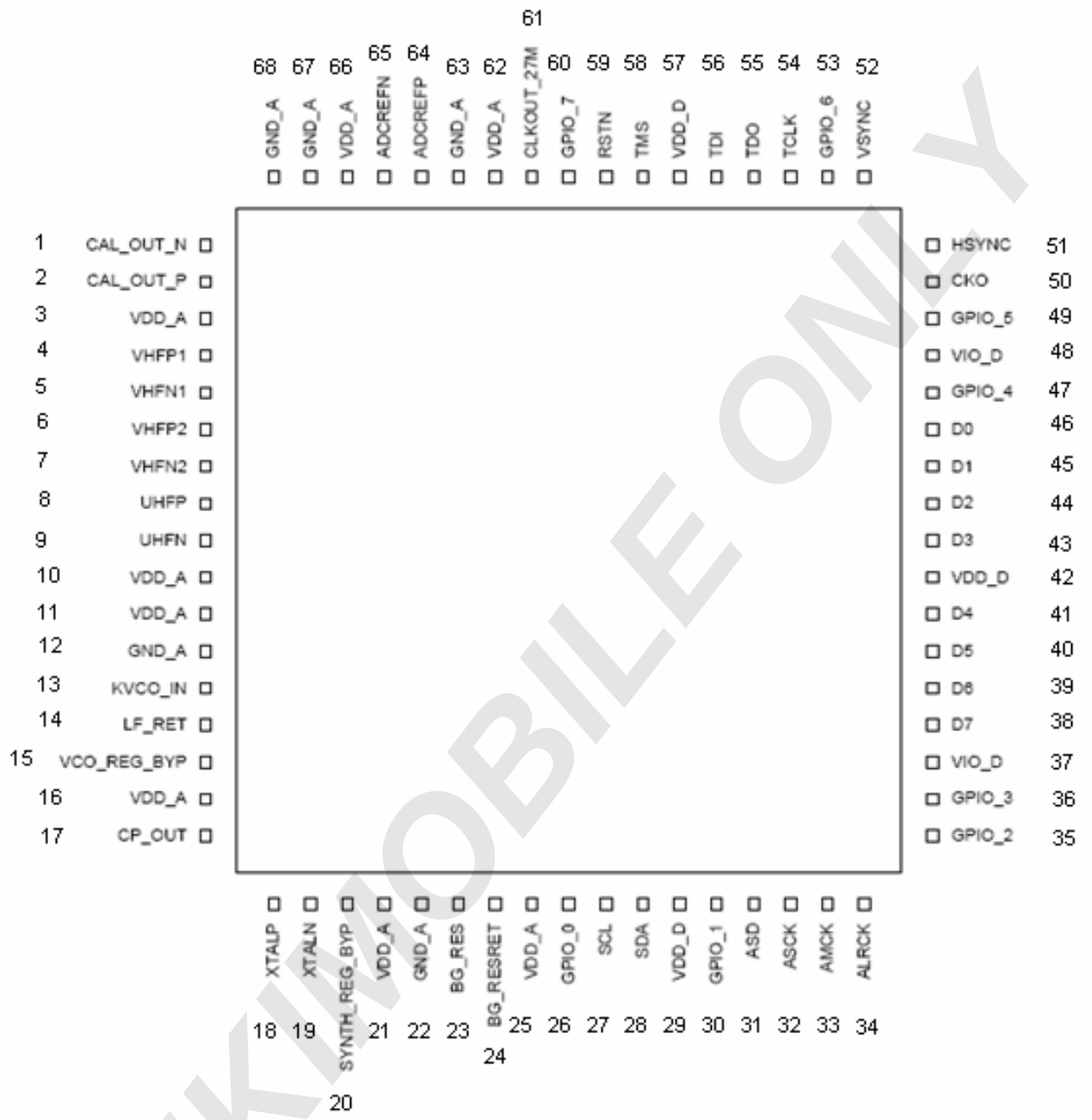
On channel change, a simplified calibration form is used to minimize the amount of time needed to change channels. The sequence of operations is:

1. Set the channel carrier frequency by programming the synthesizer to the desired value (as documented above)
2. Upon lock detect (again indicated by the lock detect bit in the master calibration register), write the associated channel seed (filt2_cal_seed<9:0>) into the FILT2_CAL register for filter cal II. This activates the final calibration for filter cal II.

RF AGC

All AGC functionality is handled within the TLG1100, greatly simplifying overall system design as compared to traditional tuners; the user only needs to set the gain target and AGC bandwidth control registers. At this point, the gain target and AGC bandwidths are independent of the channel frequency, and should be set once at startup. The calibration status register provides AGC loop unlock/error condition monitoring.

PACKAGE PINOUT



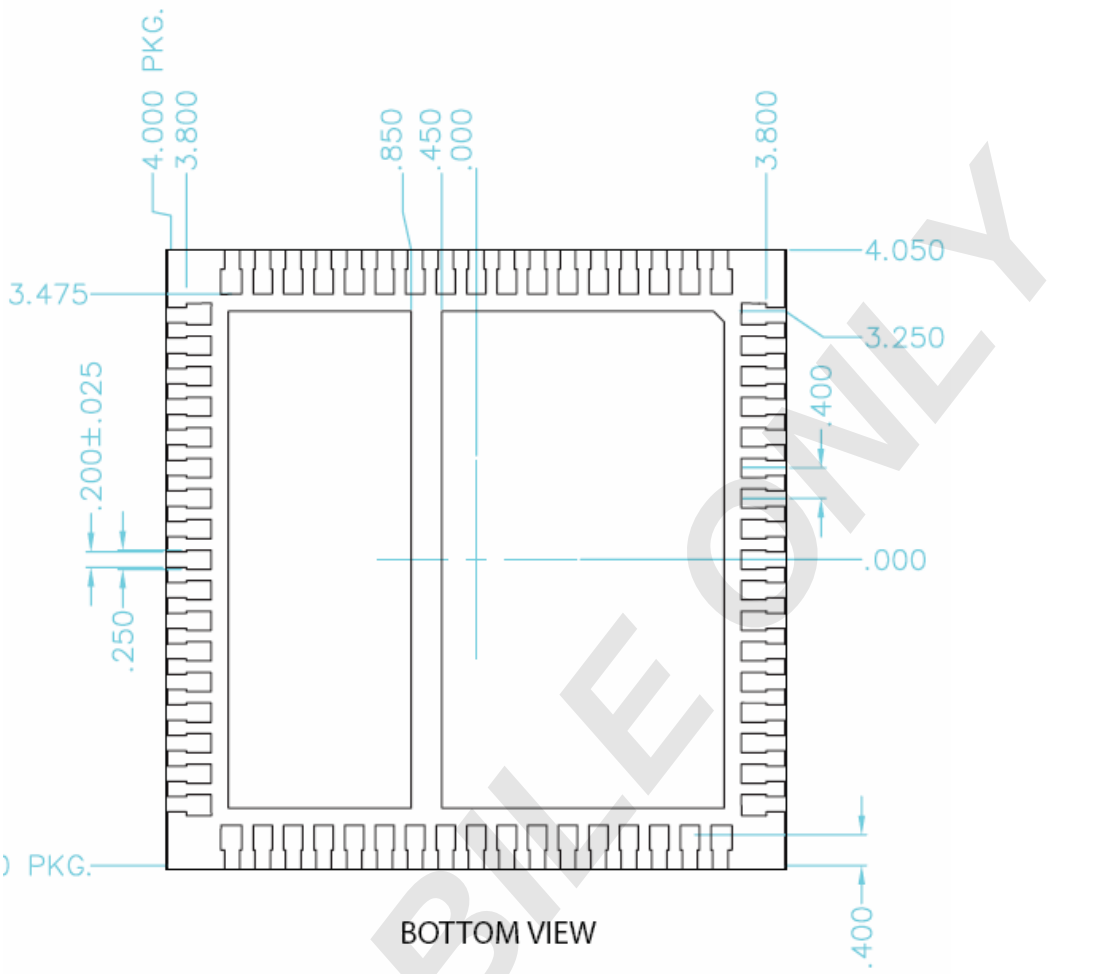
The following describes the pinout for the TLG1100, housed in a 68-pin QFN/MLF package. Note that the package has an exposed paddle for both improved grounding as well as thermal management. The paddle **must** be tied to ground; on a multilayer board, multiple vias to the ground plane is recommended.

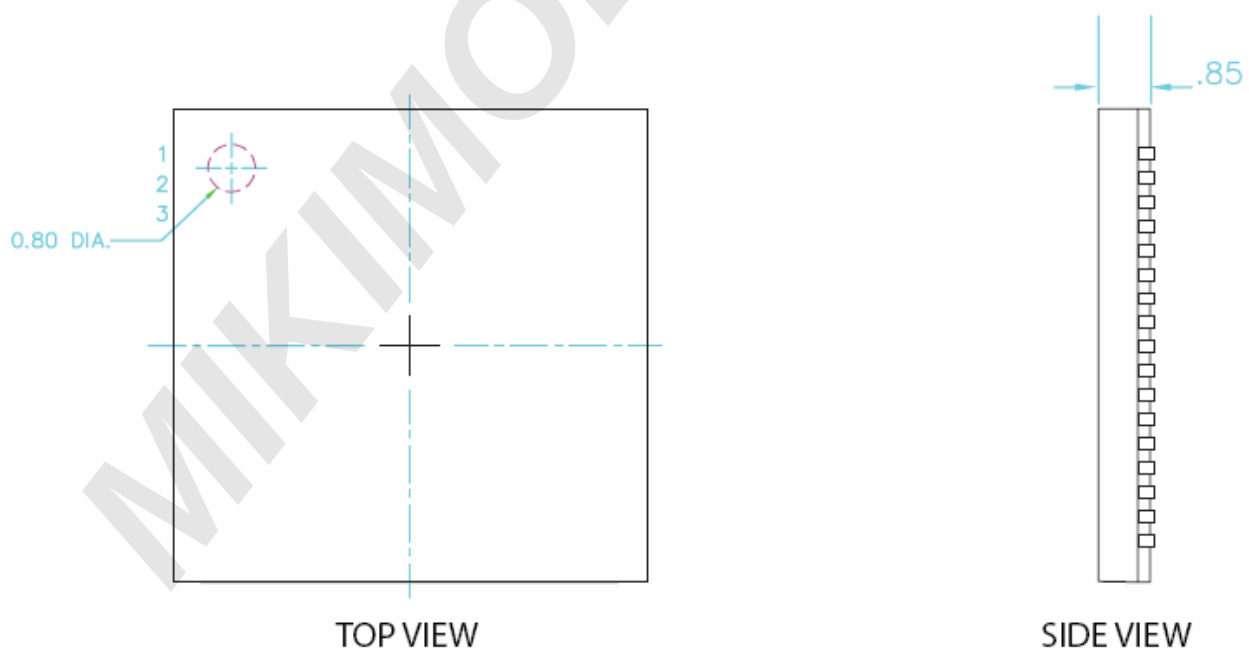
Pin #	Name	Type	Functional Description
1	CAL_OUT_N	O	Negative calibration output
2	CAL_OUT_P	O	Positive calibration output

3	VDD_A	PWR	2.8V analog VDD
4	VHFP1	I	VHF1 LNA RF input
5	VHFN1	I	VHF1 LNA RF input
6	VHFP2	I	VHF2 LNA RF input
7	VHFN2	I	VHF2 LNA RF input
8	UHFP	I	UHF LNA RF input
9	UHFN	I	UHF LNA RF input
10	VDD_A	PWR	2.8V analog VDD
11	VDD_A	PWR	2.8V analog VDD
12	GND_A	PWR	Analog ground
13	KVCO_IN	I	KVCO_IN - connected to loop filter output
14	LF_RET	I	Return reference for loop filter. DO NOT CONNECT THIS PIN TO GROUND.
15	VCO_REG_BYP	I	Internal regulator bypass pin
16	VDD_A	PWR	2.8V analog VDD
17	CP_OUT	O	Charge pump output - hook to external loop filter.
18	XTALP	I/O	27 MHz Crystal - terminal
19	XTALN	I/O	27 MHz Crystal + terminal
20	SYNTH_REG_BYP	I	Internal regulator bypass pin
21	VDD_A	PWR	2.8V analog VDD
22	GND_A	PWR	Analog ground
23	BG_RES	O	Output for external reference resistor (12k); Connect 12k resistor to BG_RESRET
24	BG_RESRET	I	Return for off-chip reference resistor. DO NOT CONNECT THIS PIN TO GROUND.
25	VDD_A	PWR	2.8V analog VDD
26	GPIO_0	I/O	GPIO 0
27	SCL	I	I2C clock
28	SDA	I/O	I2C data
29	VDD_D	PWR	1.2V core VDD for DSP
30	GPIO_1	I/O	GPIO 1
31	ASD	I/O	I2S data
32	ASCK	I/O	Audio slave clock/left sigma delta DAC
33	AMCK	I/O	Audio master clock/right sigma delta DAC
34	ALRCK	O	Left/right audio sample indicator
35	GPIO_2	I/O	GPIO 2
36	GPIO_3	I/O	GPIO 3
37	VIO_D	PWR	2.8V VDD for digital I/O's
38	D7	O	ITU/CCIR 601 data (MSB)
39	D6	O	ITU/CCIR 601 data
40	D5	O	ITU/CCIR 601 data
41	D4	O	ITU/CCIR 601 data
42	VDD_D	PWR	1.2V core VDD for DSP
43	D3	O	ITU/CCIR 601 data
44	D2	O	ITU/CCIR 601 data
45	D1	O	ITU/CCIR 601 data
46	D0	O	ITU/CCIR 601 data (LSB)
47	GPIO_4	I/O	GPIO 4
48	VIO_D	PWR	2.8V VDD for digital I/O's

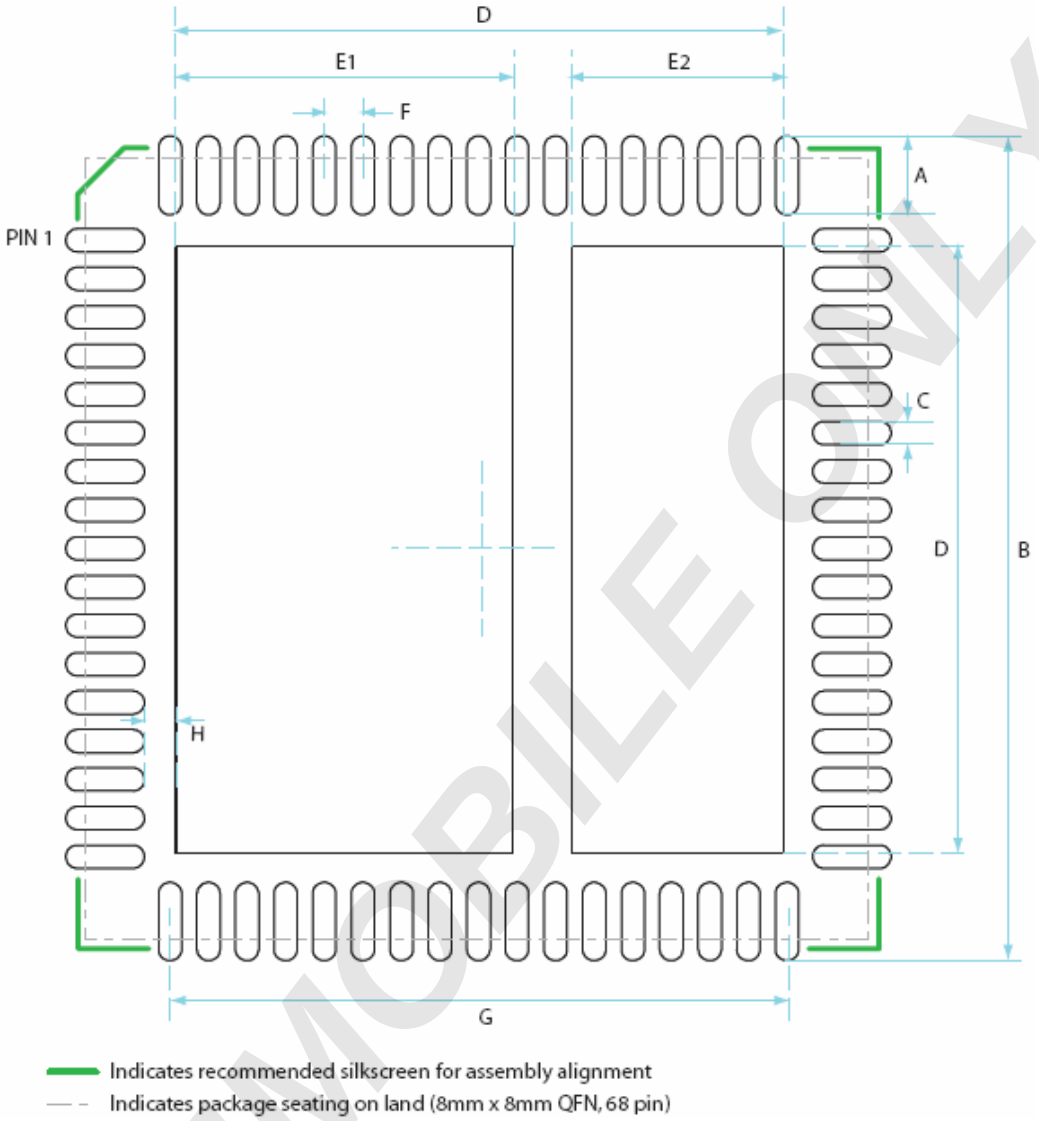
49	GPIO_5	I/O	GPIO 5
50	CKO	O	Clock output for ITU/CCIR 601 (27 MHz)
51	HSYNC	O	Hardware hsync line
52	VSYNC	O	Hardware vsync line
53	GPIO_6	I/O	GPIO 6 (switch control 1)
54	TCLK	I	JTAG clock
55	TDO	I/O	JTAG
56	TDI	I/O	JTAG
57	VDD_D	PWR	1.2V core VDD for DSP
58	TMS	I/O	JTAG
59	RSTN	I	Reset_N (ACTIVE LOW!)
60	GPIO_7	I/O	GPIO 7 (switch control 0)
61	CLKOUT_27M	O	Master clock output (normally disabled)
62	VDD_A	PWR	2.8V analog VDD
63	GND_A	PWR	Analog ground
64	ADCREFP	O	External ADC reference bypass. Connect to bypass capacitor between REFP/REFN
65	ADCREFN	O	External ADC reference bypass. Connect to bypass capacitor between REFP/REFN
66	VDD_A	PWR	2.8V analog VDD
67	GND_A	PWR	Analog ground
68	GND_A	PWR	Analog ground

PACKAGE DRAWING





RECOMMENDED LAND DIAGRAM / FOOTPRINT FOR QFN68-8x8



A	B	C	D	E1	E2	F	G	H
0.82	8.54	0.24	6.3	3.5	2.2	0.4	6.4	0.3

NOTES:
1. All units in mm.
2. Package body is centered on land (as indicated).
3. Only recommended silkscreen is for board assembly alignment / pin 1 marker.
4. Additional silkscreen at customer's discretion.
5. Solder mask should align with copper pads.
6. Note that this design is for Telegent prototype assembly use. For production, design must be adapted with regard to PCB tolerances and assembly process.
7. Exposed paddles (pins G1/G2) should be grounded. If board assembly process permits, ground vias (to ground plane) should be placed in the center of the exposed paddles.

Part Ordering Information

The table below shows the TLG1100 part ordering information.

Package Type	Part Order Number
68-pin QFN 8mm X 8mm Tray	TLG1100GC-CA

Part Marking Information

Please refer to the diagram below for TLG1100 part marking information.