

MediaTek Inc.

Confidential Information

This document is issued by MediaTek Inc. in confidence and is not to be reproduced in whole or in part without the prior written permission of MediaTek Inc. and is to be used only for the purpose for which it is submitted and is not to be released in whole or in part without the prior written permission of MediaTek Inc.

Rev. 0.1, Date: Aug. 3, 2004

MediaTek Inc.

1	Revised History	4					
2	2 Introduction						
3	Functional Description	7					
3.1	General	7					
3.2	State Timing	8					
3.3	PMIC Functional Blocks	13					
3	3.1 Charger Circuit	14					
3	3.2 LED Drivers	19					
3	3.3 Control for Backlight driver	20					
3	3.4 Diaming Control	20					
ა ვ	3.5 Dattery voltage Monitor	Z I 21					
3	3.7 DMIC Revistore	21					
3	3.8 Connection to BB	23					
4	Specifications	29					
. 4 1	Absolute maximum ratings over operating free-air temperature range	29					
4.1	Operating conditions	29					
4.3	Recommended operating specifications	29					
4.4	Regulator Output	30					
4.5	Driver output	31					
4.6	SPI switch-able Powers	32					
4.7	DIM clock	32					
4.8	Speaker Amplifier	32					
4.9	SIM Interface	32					
4.1	0 Charger Circuit	33					
5	Pin Assignment and Package	35					
5.1	Pin Assignment	35					
5.2	Package	38					
5.3	Application Example	40					
Table	1 Phone State Description	8					
Table	2 Extreme case definition	o 8					
Table	3 LDO Turn On Table	8					
Table	4 SEL 1/SEL 2 setting in each phone state	15					
Table	5 Charger State transition	16					
Table	6 Chargingcontrol	18					
Table	7 Operation for differentchargingsources	18					
Table	8 SPIdefinition	21					
Table	9 PMIC Register	23					
Table	10 Charger Status Register	23					
Table	11 Charger/Speaker Amp Control Register	24					
Table	12 LDO Status Register	24					
Table	12 D I I/D Driven Degister	_					
Table	15 K LED Driver Register	24					
Table Table	13 K LED Driver Register	24					
Table	15 K LED Driver Register	24 24 25					
Table	15 K LED Driver Register	24 24 25 25 25 25					
Table Table	15 K LED Driver Register	24 25 25 25 25 25					
Table Table Table	13 K LED Driver Register	24 24 25 25 25 25 25					
Table Table Table Table	15 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings	24 25 25 25 25 25 26 29					
Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition	24 25 25 25 25 25 26 29 29					
Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications	24 24 25 25 25 25 26 29 29 29					
Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specification s	24 24 25 25 25 26 29 29 29 29 29					
Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications	24 24 25 25 25 26 29 29 29 29 29 29 30 31					
Table Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications 25 Power Switch Specifications	24 24 25 25 25 26 29 29 29 29 29 30 31 32					
Table Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications 25 Power Switch Specifications 26 Internal DIM Clock Specifications	24 24 25 25 25 26 29 29 29 29 29 30 31 32 32					
Table Table Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications 25 Power Switch Specifications 26 Internal DIM Clock Specifications 27 Speaker Amplifier Specifications 27 Speaker Amplifier Specifications	24 24 25 25 25 26 29 29 29 29 30 31 32 32 32					
Table Table Table Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications 25 Power Switch Specifications 26 Internal DIM Clock Specifications 27 Speaker Amplifier Specifications 28 SIM Interface Specifications. 28 SIM Interface Specifications	24 24 25 25 25 26 29 29 29 29 29 30 31 32 32 32 32					
Table Table Table Table Table Table Table Table Table Table Table	13 K LED Driver Register 14 G LED Driver Register 15 B LED Driver Register 16 KP LED Driver Register 17 BL LED Driver Register 18 Miscellaneous Register 19 DIM Clock Register 20 Absolute Maximum Ratings 21 Operation Condition. 22 General Specifications 23 Regulator Specifications 24 Vibrator Driver Specifications 25 Power Switch Specifications 26 Internal DIM Clock Specifications 27 Speaker Amplifier Specifications 28 SIM Interface Specifications 29 Charger Specifications 20 Absolute the summent	24 24 25 25 25 26 29 29 29 29 29 29 30 31 32 32 32 32 33 32					

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

2/41

MediaTek Inc.

Figure1 PowerManagementStateDiagram	7
Figure2 PMICHardwareState	8
Figure3 Power key State Timing	10
Figure4 State Timing for Wake up, Paging and Stand-by	.11
Figure5 Charger State Timing	12
Figure6 ResetTiming	13
Figure7 PMICBlockDiagrams	14
Figure8 Charging states diagram	.16
Figure9 I-V curve of Li-Ion Battery Charging	18
Figure 10 LED Drivers Block Diagram	20
Figure11 LED Dimming Control	.21
Figure12 SPI Bus Timing	
Figure 13 Connection to BB	
Figure 14 Application example	40
Figure 15 BAT_ON connection with Battery Temp. sensor example	41

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

MediaTek Inc.

Revised History 1

Version	Data	Prepared by	Note
Ver. 0.1	Aug.3 2004	Chao-Chih Chiu	Initial Release

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

Commercial Confidential

MediaTek Inc.

2 Introduction

This document describes the power management IC's (hereafter called PMIC) specification including its functional requirements and electrical characteristics. 6318 supports MT621x series base band – i.e. for multimedia phone, GPRS phone and color LCD GSM only phone.

To complete a GSM/GPRS mobile handset, where power saving is a paramount issue, a device which support power related function and under proper MMI control is required, this functional block should have the following main features:

- 1. Lowdrop-out regulators.
- 2. Switching DC/DC and charge pump with high operation efficiency and low stand-by currents.
- 3. Power-on Reset and start-up timer.
- 4. Battery Charging circuits.
- 5. Thermal Overload Protection.
- 6. Under -VoltageLock-up protection.
- 7. Over-VoltageLock-up protection.

For MT621x series base band, PMIC requires following power supply voltage/current and functionality to complete a GSM/GPRS mobile handset:

- A. Power source: one 3.6V Li-ion cell.
- B. Charger for Li-ion battery (maximum input voltage 6.5V).
- C. Power-up sequencer and Protection Logic.
- D. Heven Regulator Outputs:

item	LDO	Voltage	Current	Description
1	VD	*1.8V/1.5/1.2V /**0.9V	200mA	Digital core
2	VMC	2.8V	200mA	Memory card (MS, SD, MMC)
3	VIO	2.8V	100mA	Digital IO
4	VA	2.8V	150mA	Analog and Mixed Signal
5	VSW_A	2.8V/3.3V	50mA	Auxiliary Analog circuit.
6	VRTC	*1.5/1.2V	0.2mA	Real Time Clock
7	VM	1.8/2.8V	150mA	External Memory, selectable
8	VSIM	1.8/3.0V	20mA	SIM Card, selectable
9	VTCXO	2.8V	20mA	13/26MHz reference clock
10	VUSB	3.3V	20mA	USB IO
11	VIBR	1.8V/2.8V	200mA	Vibrator

* There are bonding options for VDLDO and VRTC LDO. VD output voltage can be configured as 1.8/1.5/1.2 V options and VRTC output voltage can be configured as 1.5/1.2V options.

** VD output voltage = 0.9V (Only for VD = 1.2V option) is controlled by BB software through SPI

E. Four LED drivers

	-		
Regulator	Туре	Current	Description
LED_R	Currentregulator	12/16/20/24 mA	Drive red LED
LED_G	Currentregulator	12/16/20/24 mA	Drive green LED
LED_B	Currentregulator	12/16/20/24 mA	Drive blue LED
LED_KP	Voltagefeedback	200mA	Drive keypad LEDs
	currentregulator		

For the above regulator's output current rating, 50% margin already add up for their nominal current consumption, i.e. this means when a regulator output is required to output 150mA, the peak consumption current is 100mA. During Active state, the phone consumes peak output current at each regulator, the thermal design should consider accordingly.

F.LCD backlight white LED driver control

Only control part is implemented in this PMIC for the sake of not to use high voltage process, the external driver capability is specified as following.

Driver	Туре	Current	Description
V_BL	Switching DC/DC	80mA	Drive backlight white LEDs
	usainductor		

Confidential Information

Revision 0.1 – Aug. 3, 2004 © 2004 MediaTek Inc. 5/41

MediaTek Inc.

G. 400 mW single channel audio amplifier H. SPI 3 wires interface

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

6/41

Commercial Confidential

MediaTek Inc.

3 Functional Description

3.1 General

Power management is one of the most important functions in this PMIC. The power management function is to implement proper management procedure and control function on battery, charger and power supply in the Mobile handset. To make it clear, the management criterion is to provide the power for a mobile phone while extending the standby/active time as long as possible.

To make following description clearly understood, we first show here the operation state diagram of a typical mobile phone and the block diagram implemented in PMIC is further shown below to describe the relationships between different states.



Figure 1 Power Management State Diagram

Note the above diagram including many software activities, PMIC reacts to only part of the states and could be simplified as follows:

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc. 7/41





Figure 2 PMIC Hardware State

Table 1 Phone State Description

States	Description
Power Off	No battery connected or Battery connected but the battery was deep discharged, i.e. VBAT < 3.3V, at this state, no LDO should be enabled except VRTC. VRTC should only be disabled when VBAT<2.5V.
Switched Off	Phone was connected with battery but was switched off. The battery voltage is higher than 3.3V, at this state, VRTC was enabled, and all other LDO was disabled.
Pre-Charging	The charger was connect to mobile, but VBAT<3.3V. Slow charging is activated with charger circuits in PMIC. Upon VBAT is charged up to 3.3V, then detection circuit in PMIC will enable normal charging and pull UV signal low, also enable all LDO outputs. Charging at 50mA constant current.
Stand-by	Phone was powered up but the 13MHz reference Clock was disabled, part of Base band runs on 32K clock. At this state : LDO of VA, VTCXO, are disabled. LDO of VD, VIO, VM and VRTC are enabled.
Active	Phone was power up and running on 13MHz reference clock. All LDOs are enabled, Mobile radio task running.
Active Alarm	Phone was waked-up via RTC alarm, all LDOs were enabled, but only alarm task is scheduled, no any radio activities are scheduled.
Switched Off	The mobile has charger connected, base band is active and running on
/ Charging	13MHz reference clock but only charging software is scheduled, no any Radio nor MMI task was activated, LCD screen should only show battery charging status.
Active / Charging	The mobile has charger connected, base band is active and running on 13MHz reference clock with regular mobile radio and MMI task activated, LCD screen show battery charging status plus all normal tasks.

Table 2 Extreme case definition

Terms	Description
UV	When PWRIN<2.9V in switch on condition (active or idle). PMIC should go to

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

8/41

MediaTek Inc.

	power off state.
ov	Once Vbat > 4.3V+/-50mV (Li-ion), a hardware over voltage protection circuit (OV) should be activated to turn off charging. Charger status register D7 shall set to 1 when OV occurred. PMIC shall keep turn off charging until this bit (D7) OV was rest to 0 by BB software. Normally VBAT would not exceed 4.2V during charging, but if there is something wrong in the charging control OV can protect the battery pack from over-charged.
TRM	Thermal overload protection function, when phone is in active state and PMIC reach over-heat condition then PMIC should shut down completely.

Table 3 LDO Turn On Table

Condition										0	peration			
THR	UV (PWRIN)	CH DET	PWRK EY	PWRB B	SRCLK EN	PWRIN <2.5V	VTC XO	VRT C	VA	VD,VIO, VM	Vusb	VM C	VSIM	Vsw_a
L	Н	Х	Х	Х	Х	Н	Off	Off	Off	Off	Off	Off	Off	Off
L	Н	Х	Х	Х	Х	L	Off	On	Off	Off	Off	Off	Off	Off
L	L	L	Н	L	Х	L	Off	On	Off	Off	Off	Off	Off	Off
L	L	Н	Х	Х	Н	L	On	On	VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	Off	On	VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	Х	L	Х	Н	L	On	On	VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	$VA_SW = 0 Off$ $VA_SW = 1, VA$
					L	L	Off		VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	Х	Х	Н	Н	L	On	On	VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	$VA_SW = 0 Off$ $VA_SW = 1, VA$
					L	L	Off		VASEL/VB_OUT = 0, VA = VD VASEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR & USB_DET & ~BAT_ON	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
Н	Х	Х	Х	Х	Х	Х	Off	Off	Off	Off	Off	Off	Off	Off

During pre-charging, an external switch can be used to supply the power for LDOs (VD, VIO, VM, VRTC, VTCXO).

X means no change. Don't care.

3.2 **State Timing**

In this chapter we will describe the power on/off, wake up, charging and reset sequences in detail. For the following timing diagrams, the phone state is shown in the X-axis, Y axis shows the related signals and text in upper represents the transition events.

Confidential Information

MediaTek Inc.



Figure 3 Power key State Timing

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

10/41

MediaTek Inc.



Figure 4 State Timing for Wake up, Paging and Stand-by

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

11/41

MediaTek Inc.



Figure 5 Charger State Timing

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

12/41

MediaTek Inc.



Figure 6 Reset Timing

PMIC Functional Blocks 3.3

In order to describe each block of PMIC into detail the overall hardware block diagram of PMIC is depicted as Figure 3. More detail description for each sub-blocks will be found in the following paragraphs.

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

13/41

Commercial Confidential

MediaTek Inc.



Figure 7 PMIC Block Diagrams

3.3.1 Charger Circuit

The charger circuit in PMIC is mainly comprised of 4 sub-functions:

1. Charger detector:

Sense the charging voltage from either a standard AC-DC adaptor or USB connection, once the charging

Input voltage is greater than 4.2V will trigger the charging process. This detector should resist higher input voltage than other part of PMIC, i.e. if excess charging source detected (>6.5V) it could stop the charging process to avoid burn out the whole chip even the whole phone.

In case both AC and USB are detected, the charging source should use AC source.

Once detection of charger voltage (Either AC or USB) present, an interrupt output pin "INT" should be active (pull LOW). The "INT" is also active when AC or USB regulator was removed

The PMIC shall reset "INT" to HIGH after BB read the PMIC through SPI.

2. Charger control:

When charger is on, control the charging phase and turn on related LDOs according to the battery status. It should keep monitoring the battery voltage, if it's greater than 4.3V then stop charging immediately to keep battery from permanent damage.

Due to the process variation, the charging current may vary form chip to chip. In order to compensate this variation, an offset value (+12%--16%) will be set to PMIC. PMIC should read this compensation value and do the charging current offset when phone is in charging state. This compensation value may be calculated in phone production calibration process or always monitor by BB during phone is in charging. Offset value will be set by BB software (Register 10 bit D2~D0).

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc. 14/41

Commercial Confidential

3. USB regulator:

Regulate the charger input from USB power to 3.3V for BB (USB IO). The AC input is not use for this regulator. The V_USB 3.3V LDO output on/off should follow the control bit USB_PWR (Register Index 1 D3).

When USB regulator is unplugged or the USB_PWR control bit is set to "off", the V_USB output voltage should drop below 0.3V within 1 msec. (With V_USB output shunt with 1 uF capacitor)

The charging control should first clamp the charging current to 90mA, after the BB talk with the USB host and if the power class announced as 450mA then BB should set the register via SPI and PMIC charger will release the charging current limit to 450mA. For more detail please refer to Table 11.

BB can disable the USB task by setting the D1 (USB_PWR) of register 1 to 0 via SPI, after USB regulator shut off the USB host is virtually disconnected while the charging process should keep going as previous state. In case the phone is in switch off state before USB power inserted, then the BB should be wake up to determine the USB power class. The other case is the phone is in switch on state before USB power inserted, then the already wake up BB should also determine the USB power class for proper charging also the USB data transfer operation. MMI should allow user to utilize USB simply as charger only as described above.

4. Control for Pre-charge indication:

PMIC should provide 2 control signals (SEL1, SEL2) for the application that could show pre-charge status in LCD. In normal case VBAT is selected (SEL2 is turned on) as the power input to PMIC, while under battery low condition (VBAT<3.3V), charger source (AC) is selected (SEL1 is turned on), to substitute the power normally provided by VBAT, then allow BB powered up and at least light up the LED to show the charging status. However, if customers don't connect the two external switches and the pre-charging status will not be displayed.

SEL1 is turn on only in pre-charging state, SEL 1/SEL2 should not be turned on simultaneously in any time. During pre-charging state and when VBAT is passing 3.3V, the PMIC should handle to switch SEL1 off and SEL2 on to have the VBAT supply the whole system as normal condition.

Table 4 describes the SEL 1/SEL 2 on/off for each phone state :

Initial Phone	Initial Charging	Condition	Description	PMIC	
Not in charge	State			setting	
Switch on idle	Х	Vbat >= 3.3V	可以打電話	Select 2 on	Х
	(Not in charge)	Vbat < 3.3V	低電壓警示 per 30sec		
		Vbat = 3.3V	 軟體關機		
		PWRIN = 2.9V	PMICshutdown		
Switch on	Х	Vbat >= 3.3V	In talk		
talking	(Not in charge)	Vbat = 3.3V	Drop call → 低電壓警示		
			per 30sec		
Power off & Switch off	X (Not in charge)	x	X		
Switch on cha	raina				
Switch on talking	Normal Charge	Vbat >= 3.3V	In talk	Select 2 on	You can select a different charging
	CC mode Charge	Vbat < 3.3V	Turn back to idle		current via SPI in CC mode.
Switch on idle	Normal Charge	PWRIN >= 2.9V	In idle		
Switch off cha	rging				
Poweroff	Precharge	Vbat < 3.3V	Pre-charge & power on keydisable	Select 1 on	CC mode charging 50mA
Power off → Switch off transient	Precharge	Vbat = 3.3V	Pre-charge & power on keyenable	Select 1 off → after delay → select 2 on. (During this transient, precharge is still ongoing.	CC mode charging 50mA

Table 4 SEL 1/SEL 2 setting in each phone state

Confidential Information

Revision 0.1 – Aug. 3, 2004 © 2004 MediaTek Inc.

Commercial Confidential

MediaTek Inc.

Switch off Norma	al charge Vbat > 3.3V	Only charger task is activated.	s Select 2 on	You can select a different charging current via SPI in CC mode.
------------------	-----------------------	------------------------------------	---------------	--

When in charging the PMIC use "*GRVAC/GDRVUSB*" to control the current flow through the external MOSs, at the same time maintains the current control loop by sensing the voltage drop ("*ISENSE*") across the external current sense resistor (0.2 Ohm). Note that the charging current limit for USB is 450mA and is 800mA for AC.

Battery charging states including No Charge Mode, Constant Current (CC) Charge Mode (pre-charge, constant current), and Constant Voltage(CV) Charge Mode. No matter what status the phone is in, PMIC charger should handle the charging state transition and reflect the status in register 0 (charger status) for BB to read.



Figure 8 Charging states diagram

Table 5 Charger State transition

Current State	Transition conditions	Next State
No charge	CHRDET=1, CV=0,	CC Charge mode
	BAT_On = 0	-
	CHRDET=1,CV=1	CV Charge mode
	BAT_On = 0	_
CC charge mode	CHRDET=0	No-charge
	BAT_On=1	
	CV= 1	CV Charge
CV charge mode	CHRDET=0	No-charge
	BAT_On=1	
	CV= 0	CC Charge

Confidential Information

Revision 0.1 - Aug. 3,2004 © 2004 MediaTek Inc. 16/41

Commercial Confidential

MediaTek Inc.

Note: CHRDET is internal used bit in PMIC, which is related to USB_DET or AC_DET according to the table in below:

CHR_DET	AC_DET	USB_DET
No Charging	0	0
AC Reg. for charging	1	0
USB Reg. For charging	0	1
AC Reg. For charging	1	1
No Charging	Illegal Charger	0
No Charging	Illegal Charger	1

The BB can stop the charging by setting "*Chr_en*" to "0" via SPI interface, this means that although PMIC handle the charging process automatically, BB is the true master to manage the charging process. This control mechanism allows the BB to command the PMIC doing elegant trickling charging if necessary.

One pin called "BAT_ON" should turn off the charger immediately if it goes high (>2.45+/-0.05V). This function is designated to block the charger input in case battery is accidentally pull out. When during charging the disconnection of battery might cause the VBAT voltage surge damage the chip before the over-voltage protection turn on. BAT_ON = 1 should also shut down USB regulator in case they are turned on.

Note that "UV" is the internal signal which will equal to "1" when PWRIN < 3.2 V in, the threshold for "UV" should has a 300mv hysteresis margin in states other than pre-charge, i.e., "UV" = 1 for 2.9V<PWRIN. The reason is to avoid state bouncing back and forth between pre-charge and other states. Recall that "UV" serves as the under voltage lock up signal (refer Fig2), when UV=1 it means the battery is too weak to sustain an eligible phone call therefore PMIC should go to power off state. To provide a pleasant user interface, in switch on condition the BB should keep monitoring the battery voltage, once VBAT is lower than 3.3V MMI should issue alert sound and/or display battery low message on LCD to inform the user. For phone use this PMIC the alert sound might be any user specified chime rather than screak by traditional alerter.

The charging state is turned on/off or paused can be shown as the following table.

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc. 17/41

MediaTek Inc.

Table 6 Charging control

State	CHREN	CHRDET (CHRIN> 4.2V)	VBAT< 3.3/3.0V	CV (VBAT >4.2V)	Bat_on→BATON (batteryinsert)	Operation
No charging	X	L	х	X	L	Wait chr_det transition
Charger detection	L	Н	L	X	L	WaitCHREN
Pre-charge	X	Н	н	L	L	Monitor UV, CHRDET Note 1
CCcharge	Н	Н	L	L	L	Monitor CV, CHRDET
CVcharge	Н	Н	L	н	L	Monitor CHRDET
Pause - charging	L	Н	X	X	L	Nocharge, keepcurrent state (For BB to emulate trickle charge)
Emergent stop	x	Н	x	X	Н	Turn off charger → power off state

Note 1: The threshold of voltage to determine VBAT signal is 3.3V for pre-charge state, and 3.0V for the other states. This hysteresis is designated to prevent the state from bouncing back and forth in occasion such as surge of current demanded.



Figure 9 I-V curve of Li-Ion Battery Charging

Table 7 Operation for different charging sources

AC	USB	Phonestate	Operation	
Off	Off	Anystate	No charging.	
Confident	Confidential Information		Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.	18/41

CommercialConfidential

MediaTek Inc.

On	Off	Power off	Start pre-charge, use SEL1 to select AC charger source for PWRIN then
•	•		turn on (VTCXO, VM, VD, VIO, VA) LDOs. BB run charging management task
			to display charging state.
		Switchoff	Turn on (VTCXO, VM, VD, VIO, VA) LDOs, BB run charging management
			task to display charging state.
		Switch on	Follow normal charging procedure.
Off	On	Power off	Use USB to start pre-charge (90mA limit) and turn on USB regulator. No
			matter what power class the USB attached can provided, PMIC just charge
			the battery with constant pre-charge current. Since the BB is still off, no
			charge status is shown.
		Switchoff	Use USB as charging source. First turn on (VTCXO, VM, VD, VIO, VA) LDOs
			and USB regulator, then BB trigger USB function to determine the host's
			powerclass, after BB had set the appropriate current limit (90/450 mA) then
			PMIC start normal charging procedure and BB run charging management
			task to display charging state.
		Switch on	Use USB as charging source. First initiate USB function to determine the
			host's power class, after BB had set the appropriate current limit (90/450
			mA) then PMIC start normal charging procedure and BB run charging
			management task to display charging state.
On	On	Power off	Use AC to start pre-charge, can also use SEL1 to select AC charger source
			for PWRIN then turn on (VTCXO, VM, VD, VIO, VA) LDOs. BB run charging
			management task to display charging state. Turn on USB regulator.
		Switchoff	Use AC as charging source. Turn on (VTCXO, VM, VD, VIO, VA) LDOs to
			start normal charging procedure and BB run charging management task to
			display charging state. USB regulator is turn on also.
		Switch on	Use AC as charging source to start normal charging procedure. USB
			regulator is turn on also.

*Note the LDOs (VTCXO, VM, VD, VIO, VA) listed here are turned on/off by PMIC itself, other drivers like BL and RGB can be turned on via BB through SPI.

3.3.2 LED Drivers

PMIC provides 4 independent drivers, 3 of them uses identical structure to drive 3 different LEDs (R/G/B). The other one is dedicated to drive key pad LEDs. The reason to separate LED drivers to 2 groups is phone feature oriented. First, because of the prevailing of displaying colorful backlight when a call is coming, 3 independent drivers can easily used to mingle a lot of illuminating colors. Second, LEDs for bar type LCD and key pad normally will not turn on at the same time. Therefore a 2 step architecture is beneficial for pin count saving and power efficiency.

The first hence common block for KP and R/G/B LED drivers is a switching capacitor type DC/DC (charge pump circuit), it boost VBAT to 4.5V (note VBAT<4.2V). This charge pump circuit features driving capability control option for reduce current consumption and start-up inrush current.

KP LED driver should be a voltage feedback type regulator available to supply 200mA for up to 8 parallel KP LEDs. External ballast resistors are necessary serial connected to each LED, but only one provide the feedback voltage to PMIC. As well understood that moderate variation of light intensity for different LEDs in KP is not a critical issue. Therefore this configuration is simpler and save PMIC pin count.

R/G/B LED drivers are 3 identical current regulators, the three external LEDs connect their anodes to three pins of PMIC ("LED_R/G/B") while with their cathode connected to ground. No ballast resistor is needed for these 3 LEDs, each current regulator should be capable of setting its current to 12,16,20 or 24mA via control registers.

Confidential Information

Revision 0.1 – Aug. 3, 2004 © 2004 MediaTek Inc. 19/41

Commercial Confidential

MediaTek Inc.



Figure 10 LED Drivers BlockDiagram

3.3.3 Control for Backlight driver

This part of circuit is responsible to control the external boost DC/DC converter which is required to drive up to 6 white LEDS (2 legs, 3 in series). "BLDRV" should connect to the gate of external MOSFET, "CS_BL" is used to sense the current flow through the MOSFET and "FB_BL" feedback the voltage drop on ballast resistor for LED light intensity control. "DC_OV" is to prevent the over-voltage of output.

3.3.4 Dim ming Control

Brightness can be controlled by programming 6318's internal registers to change the driver's output pulse duty cycle and frequency.

Pulse duty cycle:

For all drivers, the output duty cycle is adjusted by selecting the corresponding driver's PWM_D value according to the following relationship:

 $(\bar{R}/G/B/KP)$ PWM duty cycle = $(PWM_D + 1)$ low 's, and 32 - $(PWM_D + 1)$ high's.

, where PWM_D ranges from 0 to 31.

Frequency:

For R/G/B and KP, the output frequency is adjusted by adjusting Register 9 [3:0] DIV value. These 4 LED drivers share the same DIV setting. The output frequency is governed by:

(R,G,B,KP) PWM frequency = 800k/25/(DIV +1)/32 , where DIV ranges from 0 to15

For BL, the output frequency is adjusted by adjusting Register 9 [7:4] BL_DIV value and also Register 7 [5] bypass value. The output frequency is governed by:

when bypass = 0,

(BL) PWM frequency = 800k/25/(BL_DIV +1)/32

Confidential Information

Revision 0.1 - Aug. 3,2004 © 2004 MediaTek Inc. 20/41

Commercial Confidential

MediaTek Inc.

when bypass = 1, (BL) PWM frequency = 800k/(BL_DIV +1)/32 , where BL_DIV =0~15

Figure 11 LED Dimming Control

3.3.5 Battery Voltage Monitor

PMIC features to output either VBAT or ISENSE voltage or to VB_OUT pin. In addition, divided by two option is support. This function facilitate baseband chip to monitor VBAT and/or ISENSE voltage to control the charger process.

3.3.6 SPI interface

PMIC uses 3 wire interface to connect to BB. This bi-directional serial bus interface allows BB to write command to and read status from PMIC. The bus protocol utilizes a 16 bits proprietary format, the description for the 3 signals are listed as following table.

Table 8 SPIdefinition

Signal Name	Attribute	Direction	Description
SPICK	Edge trigger	BB→PMIC	Serial bus clock
SPIDAT	Level	$BB \leftrightarrow PMIC$	Serial data
SPICS	Active low	BB→PMIC	PMIC SPI bus selection

Once SPICS goes low, this bus is active, BB start to transfer the 4 register index bits followed by a read/write bit, then wait for 3 clock for PMIC SPI state machine to decoded the operation for succeeding 8 data bits. The state machine should count for 16 clocks to complete the data transfer, if there are less than 16 clocks received during SPICS = 0 then just part of the data been transferred, on the other hand if more than 16 clocks received then the extra data will be ignored.

The first SPICK will be started 100 nsec after the SPICS is asserted low.

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc. 21/41

MediaTek Inc.



*Read = BB reading from PMIC, Write= BB writing to PMIC Figure 12 SPI Bus Timing

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

22/41

MediaTek Inc.

3.3.7 **PMIC Registers**

There are 10 registers in PMIC for the purpose to receive BB commands and reflect PMIC status.

Table 9 PMIC Register

Index	Name	D7	D6	D5	D4	D3	D2	D1	D0
0	Charger	OV_SPI	CHRDET	BAT_ON	AC_DET	USB_DET	Pwrkey_deb	CV	CHR G_DIS
-	Status	R	R	R	R	R	Ŕ	R	R
1	Charger /	CHREN	AMPGAIN 2	AMPGAIN 1	AMPGAIN 0	USB PWR	CLASS D2	CLASS D1	CLASS D0
	Speaker	RW	RW	RW	RW	RW	RW	RW	RW
	Control	1	0	0	0	0	0	0	0
2	LDO	VD	νĂ	VM	VRTC	ντζχο	VŠIM	Rese	ved
-	Status	P	P	P	P	P	P	1000	·ou
	olaluo	IX.	IX I	IX IX	IX.	IX I	IX I		
2	BIED	On	CURLIM4						
3	Driver								
	Dilvei	R W	RVV 0	R W	R VV	<u>RW</u>	<u>R</u> VV	R VV	R W
-		0							
4	GLED	On	CURLINI	CURLINU	PVVIVI_D4	PVVIVI_D3			
	Driver	RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
5	B LED	On	CURLIM1	CURLIMO	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
	Driver	RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
6	KP LED	On	Rese	rved	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
	Driver	RW			RW	RW	RW	RW	RW
		0	1		0	0	0	0	0
7	BL LED	On	Reserved	bypass	PWM D4	PWM D3	PWM D2	PWM D1	PWM D0
-	Driver	RW	-	ŔŴ	RŴ	RŴ	RŴ	RŴ	RŴ
		0	1	0	0	0	0	0	0
8	Miscel laneo	CHR_PUMP_EN	VA SW	Pwr save	Vasel	VMC	VSIMSEL	SPEAKER	VIBRATOR
•	us	RW	RW	RW	RW	RŴ	RW	RW	RW
		0	1	0	0	0	0	0	0
9	DIM clock	BL DIV3	BL DIV2	BL DIVI	BL DIVO	DIV 3	DIV 2	DIV 1	DIV 0
°.		RW		RW	RW	RW	RW	RW	RW
	1	0	0	0	0	0	0	0	0
٨	Charger	0	Res	arved	Ū	Ov spi clr	Chofst[2]	Chofst[1]	Chofst[0]
~	ctrl2		nes.				RVV	P///	RVV
	CUTZ					٧V	0	1	1
D	Bandgan	Pcol1	Pcol0	Occon	ckcol	lco11		Poso	nvod
Р	Sotting	DW	DW	DW	DW		DW	Rese	veu
	Jeung	RW	RW	RW	RW	RW	RW		
	DO TESTA	0	0	0	U	U	0		
C					Reser	ved			
	Γ'								
_		_							
D	LDO_TEST2	Rese	rved	Int_drv	Reset_drv		Rese	rved	
	EN			RW	RW				
				1	1				
E	Charge	pumpclctrl	Pumpdsel_1	Pumpdsel_0	Pumpssel_1	Pumpssel_0	Dc_sel	vibsel	Usb_chren
	pump ctrl	RW	RW	RW	RW	RW	RW	RW	RW
		0	1	1	0	0	0	0	1
F	Extras	Vsw_a_sel	Vbssel_spi[1]	Vbssel_spi[0]	Vbhsel	Reserved	SimIstype	Pumpdelay[1]	Pumpdelay[0]
		RW	RW	RW	RW		RW	RW	RW
		0	0	0	0		0	1	1

Table 10 Charger Status Register

	Register Index 0: Charger Status (R only)					
Bit	Name	Value	Description			
D7	(R/W) OV	0	OV has not occurred			
		1	OV has occurred, need to wait for BB to clear			
D6	CHRDET	0 Charger not detected				
		1	Charger detected			
D5	BAT_ON	0 Battery is connected				
		1	Battery is not connected			
D4	AC_DET	0	AC power not detected			
		1	AC power detected			
D3	USB_DET	0	USB power not detected			
		1	USB power detected			
D2	PWRKEY_DEB	0	Debounced pwrkey is asserted.			
		1	Debounced pwrkey is not asserted.			

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

23/41

MediaTek Inc.

D1	CV	0	Not in CV mode.		
		1	In CV mode.		
D0	CHRG_DIS	0	Charging.		
		1	Not charging.		
Note: If CV	Note: If CV = 0, and CHARG_DIS=0, then this implies that it is in CC mode.				

Table 11 Charger/Speaker Amp Control Register

	Register Index 1: Charger /Speaker Control					
Bit	Name	Value	Description			
D7	CHREN	0	Pause charging			
		1	Enable charging (Default)			
D6~D4	AMPGAIN[2:0]	0~7	Speaker Amplifier Gain setting 0~14 dB (Default = 000)			
D3	USB_PWR	0	Turn off USB regulator (Default)			
		1	Turn on USB regulator			
D2~D0	CLASS_D(2:0)	0	Charge current clamp to 50mA			
		1	Charge current clamp to 90mA			
		2	Charge current clamp to 150mA			
		3	Charge current clamp to 225mA			
		4	Charge current clamp to 300mA			
		5	Charge current clamp to 450mA			
		6	Charge current clamp to 650mA			
		7	Charge current clamp to 800mA			

Table 12 LDO Status Register

	Register Index 2: LDO Status (R only)						
Bit	Name	Value	Description				
D7	VD	0	Digital LDO off				
		1	Digital LDO on				
D6	VA	0 Analog LDO off					
1 Analog LDO on							
D5	VM	0	Memory LDO off				
		1	Memory LDO on				
D4	VRTC	0	RTC LDO off				
		1	RTC LDO on				
D3	VTCXO	0	13/26 MHZ VTCXO LDO off				
		1	13/26 MHZ VTCXO LDO on				
D2	VSIM	0	SIM LDO off				
		1	SIM LDO on				
D1~D0	Reserved						

Table 13 R LED Driver Register

	Register Index 3: R LED Driver					
Bit	Name	Value	Description			
D7	On	0	Power down (Default)			
		1	Power On			
D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)			
		1	Current limit = 16 mA			
		2	Current limit = 20mA			
		3	Current limit = 24mA			
D4~D0	PWM_D(4:0)	0~31	Duty cycle =(PWM_D(4:0)+1)/32 (Default = 0)			

Table 14 G LED Driver Register

Register Index 4: G LED Driver				
Bit	Name	Value	Description	
D7	On	0	Power down (Default)	
		1	Power On	
Confidential Information			Revision 0.1 – Aug. 3,2004	24/41

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

24/41

MediaTek Inc.

D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)
		1	Current limit = 16 mA
		2	Current limit = 20mA
		3	Current limit = 24mA
D4~D0	PWM_D(4:0)	0~31	Duty cycle =($PWM_D(4:0)+1$)/32 (Default = 0)

Table 15 B LED Driver Register

	Register Index 5: B LED Driver				
Bit	Name	Value	Description		
D7	On	0	Power down (Default)		
		1	Power On		
D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)		
		1	Current limit = 16 mA		
		2	Current limit = 20mA		
		3	Current limit = 24mA		
D4~D0	PWM_D(4:0)	0~31	Duty cycle =($PWM_D(4:0)+1$)/32 (Default = 0)		

Table 16 KP LED Driver Register

	Register Index 6: KP LED Driver					
Bit	Name	Value	Description			
D7	On	0	Power down (Default)			
		1	Power On			
D6~D5	Reserved					
D4~D0	PWM_D(4:0)	0~31	Duty cycle = $(PWM_D(4:0)+1)/32$ (Default = 0)			

Table 17 BL LED Driver Register

Register Index 7: BL LED Driver				
Bit	Name	Value	Description	
D7	On	0	Power down (Default)	
		1	Power On	
D6	Reserved			
D5	BYPASS	0	No bypass (Default)	
		1	Bypass divide-by-25 counter.	
D4~D0	PWM_D(4:0)	0~31	Duty cycle =($PWM_D(4:0)+1$)/32 (Default = 0)	

Note:

when bypass = 0,

PWM frequency = 800k/25/(bl_div+1)/32 , div=0~15

when bypass = 1, PWM frequency = $800k/(bl_div + 1)/32$, div=0~15

Table 18 Miscellaneous Register

	Register Index 8: MiscellaneousDriver				
Bit	Name	Value	Description		
D7	CHR_PUMP_EN	0			
			Power down (Default)		
		1	Power on		
D6	VA_SW	0	Auxiliary Analog output switch off		
		1	Auxiliary Analog output switch on (Default)		
D5	PWR_SAVE	0	VD = Normal Voltage output (Default)		
		1	VD = 0.9V When in Sleep Mode		
D4	VASEL	0	VA enable signal determination, same as VD(Default)		
		1	VA enable signal determination, same as VTCXO		
D3	VMC	0	VMC power off (Default)		
		1	VMC power on		
D2	VSIMSEL	0	VSIM = 1.8V (Default)		
		1	VSIM = 3.0V		
D1	SPEAKER	0	Audio amplifier power off (Default)		
		1	Audio amplifier power on		

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

25/41

Commercial Confidential

MediaTek Inc.

D0	VIBRATOR	0	Vibrator driver power off (Default)
1		1	Vibrator driver power on

*When turn on VA_SW is the same as VA. Application like use this pin to provide power for external photo sensor can save power by making this pin floating.

**When turned on VB_OUT is actually same as VBAT. VB_OUT is floating when phone is switched off in order to stop current leak to BB.

Table 19 DIM Clock Register

Register Index 9: DIM Clock					
Bit	Name	Value	Description		
D7~D4	BL_DIV	15~0	Backlight frequency division control (Default=0)		
D3~D0	DIV	15~0	R,G,B,KP frequency division control (Default=0)		

Table 20 Charger Control_2 Register

Register Index A: Charger Control 2					
Bit	Name	Value	Description		
D7~D4	Reserved				
D3	OV_SPI_CLR	0	When written with 0, clears OV condition.		
	(W only)	1	No effect.		
D2~D0	Chofst[2:0]	7~0	Charging current offset. (Default is b'100 = 4)		

Note:

When OV_SPI_CLR is written with a 0, it clears the ov_spi condition.

Writing with a 1, has no effect.

If read, it returns the same value as bit 7 of Register 0 (ov_spi).

Table 21 Bandgap Setting Register

	Register Index B: Bangap Setting				
Bit	Name	Value	Description		
D7~D6	RSEL[1:0]	0	Bandgap Setting (Default)		
		1			
D5	OSCEN	0	Bandgap Setting (Default)		
		1			
D4	CKSEL	0	Bandgap Setting (Default)		
		1			
D3~D2	ISEL[1:0]	0	Bandgap Setting (Default)		
		1			
D1~D0	RESERVED				

Table 22 LDO Test 1 En Register

Register Index C: LDO TEST1 EN					
Bit	Name	Value	Description		
D7~D0	Reserved				

Table 23 LDO Test 2 En Register

Register Index D: LDO TEST2 EN						
Bit	Name	Value	Description			
D7~D6	Reserved					
D5	INT_DRV	0	Set Interrupt pad driving strength (Default = 1)			
		1				
D4	RESET_DRV	0	Set Reset pad driving strength (Default = 1)			
		1				
D3~D0	Reserved					

Table 24 Charge Pump Register

Register Index E: Charge Pump Control

Confidential Information

Revision 0.1 - Aug. 3, 2004 © 2004 MediaTek Inc. 26/41

MediaTek Inc.

Bit	Name	Value	Description
D7	PUMPCLCTRL	0	Charge Pump Control Signal (Default = 0)
		1	
D6~D5	PUMPDSEL[1:0]	3~0	Charge Pump Control Signal (Default = b'11 = 3)
D4~D3	PUMPSSEL[1:0]	3~0	Charge Pump Control Signal (Default = 0)
D2	DC_SEL	0	DC – DC select
		1	
D1	VIBSEL	0	Vibrator select
		1	
D0	USB_CHREN	0	Disable USB charging. For OTG.
		1	Enable USB charging (Default)

Table 25 Extras Register

Register Index F: Extras					
Bit	Name	Value	Description		
D7	VSW_A_SEL	0	Vsw_a = 3.3V (Default)		
		1	Vsw_a = 2.8V		
D6~D5	VBSSEL_SPI[1:0]	0~3	Vbout select (Default = 0)		
D4	VBHSEL	0	Vbout select (Default = 0)		
		1			
D3	RESERVE				
D2	SIMLSTYPE	0	Sim Level Shifter type select (Default = 0)		
		1			
D1~D0	PUMPDELAY[1:0]	3	Charge pump softstart time delay = 600us (Default = 3)		
		2	Charge pump softstart time delay = 500us		
		1	Charge pump softstart time delay = 400us		
		0	Charge pump softstart time delay = 200us		

Note:

-

Charge pump delay is controlled as follows:

When $Chr_pump_en = 1$,

after pumpdelay (200, 400, 500, or 600 us), pumpdsel will change from the default value (b'11) to the new pumpdsel value.

When Chr_pump_en =0, or reset is asserted, pumpdsel will change back to default b'11 value.

- Vbssel_spi – this is used to control the VBOUT selection.

Vbssel_Spi	vbssel (actual signal to analog)
00	00
01	01
10	10

10	
00	

Connection to BB 3.3.8

11

Following schematic illustrate a typical application for this PMIC to connect with 621X BB. Please refer to application paragraph for other possible connections.

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

27/41



Figure 13 Connection to BB

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

28/41

MediaTek Inc.

Specifications 4

Absolute maximum ratings over operating free-air temperature range 4.1

Table 20 Absolute Maximum Ratings

Parameter	Conditions	Min	Тур	Max	Units
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
ESD robustness		2000			v
Charger input withstand				9	v

Operating conditions 4.2

Table 21 Operation Condition

Parameter	Conditions	Min	Тур	Max	Units
Operatingtemperaturerange		-25		85	°C

Recommended operating specifications 4.3

Table 22 General Specifications

Items	Requirement	Unit	Notes
Switch off mode Supply Current			
VBAT <2.5V	TBD	uA	
2.5V< VBAT <3.3V		uA	
3.3V< VBAT		uA	
Operation Supply Current			
All Out puts on	TBD	uA	
VTCXO off, all others on		uA	
VA,VTCXO off, all others on		uA	
UV,			
Under Voltage ON Threshold	3.225	V	Max
	3.175	V	Min
Under Voltage Hysteresis	0.3	v	
Reset Generator			
Outnut High	Vio -0. 5	V	Min
Output Low	0.2	V	Max
Output Current	1	mA O(F	
On Delay time per Can.	2.0	mS/nF	
Off Delay		1113	
Power Key input			
High Voltage	0.7xVBAT	V	
Low Voltage	0.3xVBAT	V	
Control Input voltage			
DWDRR pin High/Low Voltage	1.0 / 0.2	v	
All other pin High/Low Voltage	2.0 / 0.5	v	
An other pin high/Low voltage			
I nermai Snutdown	150	degree	
Threshold	25	degree	
		acgree	

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

29/41

MediaTek Inc.

Hysteresis			
LDO Enable response time	250	µsec	VA, VTCXO
Within 3% of Vo	5	msec	Others

Regulator Output 4.4

Table 23 Regulator Specifications

Charge Pump Regulator				For KP and RGB LED
Output Ripple		+/- 50	mV	drivers
Efficiency		70	%	@lout=150mA.Vout=4.5V
Switching Frequency		800	KHz	
Output Current		300	mA	
output ourrent				
Power down current		10	uΑ	TBD
(CP power down?)				
No Load		1	mA	
Response Time: Rising		100	uS	10mA to Max lout
Falling		100	uS	Max lout to 10mA
Start-up time		5	mS	
Feedback voltage		200	mV	
DC/DC converter				
Maximum switch current		TBD	mA	
Efficiency		85	%	(6 LEDs load)
Switch off time		400	ns	(PWM 7-800KHz)
Switch on time			ns	TBD
Switching Free		TBD	KH7	(8mA load 4 2V/3 3V)
Voltage reference for		(220)	mV	Current limiting 468mA
current limit setting		(220)		(P=0.47 obm)
rosistor		(400 mV)	mV	(K=0.47 01111)
Foodbook voltogo		(4001114)		
Digital Care Voltage				
Output Voltage	VD	1.2 /1.5/1.8	v	1.2V= min.1.10V, max 1.30V
output (onuge	•_•		-	1.5V= min.1.40V, max 1.60V
				1.8V= min.1.70V, max 1.90V
Max. Output Current	ld-max	200	mA	
Line Regulation		5	mV	
Load Regulation		10	mV	
Digital IO Voltage				
Output Voltage	V IO	2.8	v	2.8V= min.2.70V. max 2.90V
Output Current	lio-max	100	mΑ	,, _,
Line Regulation	no max	5	mV	
Load Regulation		10	mV	
Analog Voltage		10		
Output Voltage	VΔ	28	v	2.8V= min.2.70V, max 2.90V
Output Voltage	V_A	150	mΔ	2.0V - Mill.2.1 0V, Max 2.00V
Line Degulation		5	mV	
Line Regulation		10	mV	
Output Noise Voltage		50	uVrme	f – 10 Hz to 100 kHz
Dipple Dejection		50	dB	10 Hz < Freq < 3KHz
Kippie Kejecuon		۵5 ۵۵	dB	3KHz < Freq. < 1 MHz
VTCVO Voltege		40		
Output Voltage		20	v	$2.8 \text{ //} = \min 2.70 \text{ //} \max 2.00 \text{ //}$
Output voltage		2.ŏ	v m A	2.0v= mm.2.70v, max 2.90v
Line Degulation	ncxo-	20	mV	
Line Kegulation	IIIdX	3	mV	
Loau Regulation		2	111 V	
1			1	

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

30/41

MediaTek Inc.

Output Noise Voltage		50	uVrms	f = 10 Hz to 100 kHz
Ripple Rejection		65	dB	10 Hz < Freq. <3KHz
		40	dB	3KHz < Freq. < 1 MHz
RTC Voltage				
Output Voltage	V_RTC	1.5/1.2	V	1.5V= min.1.30V, max 1.65V
Output Current Limit	I_RTC-	1.0	mA	
Off Reverse Input Current	max	1	uA	
External Memory Voltage				
Output Voltage	VМ	1.8 / 2.8	V	1.8V= min.1.70V,max1.90V
L B	_			2.8V= min.2.70V, max 2.90V
Output Current	I M max	150	mA	
Line Regulation		5	mV	
Load Regulation		10	mV	
SIM Voltage				
Output Voltage	V SIM	1.8 / 3.0	v	1.8V= min.1.71V, max 1.89V
output (onuge			-	3.0V= min.2.82V, max 3.18V
Output Current	Isim-max	20	mA	
Line Regulation		3	mV	
Load Regulation		2	mV	
Memory Card Voltage		-		
Output Voltage	V MC	28	v	2.8V= min.2.70V. max 2.90V
Output Current	L mc-	200	mΔ	,,,,
Line Degulation	max	5	mV	
Line Regulation	max	10	mV	
KD L FD		10	111 V	
Output Voltage	VKP	13	v	
Output Voltage		4.J 200	m A	Maximum
Output Current	1_131	200		
D/C/R I FD				
Output Voltage	V RGB	4.0	v	Maximum
Source Current		0	m A	Maximum
Clamp Current Accuracy	I_N/G/B	24	0/	For all 4 steps 12,16,20,24
Clamp Current Accuracy		10	70	mA
USB Voltage				
Output Voltage	V_USB	3.3	V	3.3V=min 3.15, max=3.45 V
Output Current	I_USB	20	mA	Maximum
Auxiliary Analog Voltage				
Output Voltage	VSW_A	2.8V/3.3	V	2.8V=min 2.70, max=2.90 V
				3.3V=min 3.15, max=3.45 V
Output Current	I_SWA	50	mA	Maximum
Vibrator Voltage				
Output Voltage	V_VIBR	1.8V/2.8	V	1.8V=min 1.70, max=1.90 V
				2.8V=min 270, max=290 V
Output Current	I_VIBR	200	mA	Maximum

4.5 **Driver output**

Table 24 Vibrator Driver Specifications

Item	Max	Typical	Min	Unit	Note
Output Voltage		1.8/2.8		V	Min=2.7V Typ=2.8V Max=2.9V
Output Current		250		mA	Min=1.7V Typ=1.8V Max=1.9V
Line Regulation		TBD			
Load Regulation		TBD			

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

31/41

MediaTek Inc.

SPI switch-able Powers 4.6

Table 25 Power Switch Specifications

Switch	Max	Typical	Min	Unit	Note
VB_OUT					VBAT for BB ADC
Turn on delay		TBD		us	
Turn off delay		TBD		us	
VSW_A					Auxiliary Analog voltage
Turn on delay		TBD		us	
Turn off delay		TBD		us	

4.7 **DIM clock**

Table 26 Internal DIM Clock Specifications

Item	Max	Typical	Min	Unit	Note
Internal Dim clock		30k		Hz	+/- 30% accuracy

4.8 **Speaker Amplifier**

Table 27 Speaker Amplifier Specifications

Item	Max	Typical	Min	Unit	Note
RMS Power		400		mW	@8 Ohm load, VBAT=3.4V
THD + N	0.3			%	@1kHz, P₀=0.15Wrms @3.4V
PSSR		65		dB	From 20 ~1KHz
Shutdown Current	1			uA	Bit "SPEAKER On" = 0
Quiescent Power Supply	3.5			mA	VBAT = 4.2V, no input
Current					
Gain adjustment	14		0	dB	
Gain adjustment steps	2.2	2	1.8	dB	Please see table 9 PMIC register
_					index 1. Charger/Speaker control

4.9 **SIM Interface**

Table 28 SIM Interface Specifications

Parameter	Symbol	Conditions	Min	Тур	Max	Units
VSIM	3V	lload=6mA	2.82	3	3.18	v
	1.8V	lload=6mA	1.71	1.8	1.89	v
Interface to MT	621X					
RST,CLK,I/O	Vil,Vol				0.2*VIO	v
	Vih,Voh		0.7*VIO			v
Interface to 3V	SIM card					
RST	Vol	l=-200uA			0.4	v
	Voh	l=200uA	0.9*VSIM			v
CLK	Vol	l=-20uA			0.4	v
	Voh	l=20uA	0.9*VSIM			v
I/O	Vil	l=1mA			0.4	v
Confidential Informati	ion	Revision 0.1 – Aug. 3,2004			32	2/41

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

32/41

MediaTek Inc.

	Vih	l=20uA	0.7*VSIM		v
	lil	Vil=0V		1	mA
	Vol	l=1mA		0.4	v
	Voh	l=20uA	0.8*VSIM		v
Interface to 1.8V S	IM card				
RST	Vol	l=-200uA		0.2*VSIM	v
	Voh	l=200uA	0.9*VSIM		v
CLK	Vol	I=-20uA		0.2*VSIM	v
	Voh	l=20uA	0.9*VSIM		v
I/O	Vil	l=1mA		0.2*VSIM	v
	Vih	l=20uA	0.7*VSIM		v
	lil	Vil=0V		1	mA
	Vol	l=200uA		0.4	v
	Voh	l=20uA	0.8*VSIM		v
Timing					
RST,I/O rise/fal time	l Tr/Tf	VSIM=3/1.8V, RST,I/O loaded with 30pF		1	us
CLK rise/fall time	Tr/Tf	VSIM=3V, CLK loaded with 30pF		18	ns
		VSIM=1.8V CLK loaded with 30pF		50	ns
CLK frequency	Fclk	CLK loaded with 30pF	5		MHz
CLK duty cycle	Duty		47	53	%

4.10 Charger Circuit

Table 29 Charger Specifications

Items	Symbol	Conditions	Min	Тур	Max	Unit
Charger input voltage			4.2		6.5	V
Charger detect on threshold	Vchg_on			Vbat + (0.25V)	6.5	v
Maximum charging current (USB charging)				450		mA
Maximum charging current (AC charging)				0.16/Rse nse		А
Pre-charging current				50		mA
Pre-charging off threshold				3.2		۷
Pre-charging off hysteresis				0.3		v
CC mode to CV mode threshold			4.15	4.2	4.25	v
BAT_ON	Vil				2.4	v
	Vih		2.5			V
BAT_ON / OV GATDRV rising time	Tr	CHRIN 5V, Cl 2nF	1		5	uS
CC mode charging GATDRV falling time	Tf			1		mS
Over voltage protection threshold	ov		4.25	4.3	4.35	v

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

33/41

MediaTek Inc.

Over	voltage	protection			
hysteresis				0.2	V

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

34/41

MediaTek Inc.

Pin Assignment and Package 5

5.1 **Pin Assignment**



Table 30 Pin Assignment

Pin	Symbol	Input(I)	Function				
		Analog(A)					
Control							
10	PWRKEY	I	On button input, low active				
49	PWRBB	1	Power On/Off from microprocessor, high active				
			VTCXO and VA enable, Low=disable,				
44	SRCLKEN	1	High=enable.				
45	SIMVCC	I	VSIM enable: Low=disable, High=enable				
			Indication Li-ion (Low) battery inserted, high				
47	BAT_ON	I	active				

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

35/41

MediaTek Inc.

			DC/DC protection input, OV threshold voltage is
56	DC_OV	I	1V.
			External memory supply selection, $1 = 2.8v$, $0 =$
25	VMSEL	I	1.8V
Charger con	trol		
6	AC	IA	AC-DC adaptor input
4	USB	IA	USB power input
3	V_USB	OA	3.3V USB power output
46	INT	ο	Interrupt PIN, active high. This pin is to inform BB if AC or USB regulator voltage is detected, OV occurred and BAT_On=1 Will be reset to normal low, after BB had communicated with PMIC through SPI.
			Control output to gate of external p-channel FET
5	GDRVUSB	OA	for USB charger
			Control output to gate of external p-channel FET
7	GDRVAC	OA	for AC charger
8	ISENSE	OA	Charge current sense input
			Control output to gate of external PMOS for AC
11	SEL1	OA	charger input as power source.
			Control output to gate of external PMOS for
12	SEL2	OA	VBAT input as power source.
SIM interface			
28	SIMIO	I/O	Non level shifted SIM data (3V)
29	SIMRST	I	Non level shifted SIM reset input (3V)
30	SIMCLK	I	Non level shifted SIM clock input (3V)
33	SIO	I/O	Level shifted SIM data (1.8/3V)
32	SRST	0	Level shifted SIM reset output (1.8/3V)
31	SCLK	0	Level shifted SIM clock output (1.8/3V)
Reset			
50	RSTCAP	IA	Reset delay time capacitance
43	RESET	0	System reset, low active
Power relate			
9	VBAT	IA	Battery input voltage
-	PWRIN	14	Power input
14		04	Battery output voltage switch-able
13	BP/Vref		Band pass canacitance
15 10 53 57	GND		Ground
27		0.4	Digital core supply
30	VIO		Digital IO supply
3 <u>9</u> 17			Analog supply
31			Auxiliary Analog supply
J+ 10			TCYO supply
10			
24 07			SIM supply
21 25			
33 20			
20		UA	wemory card supply
wiscellaneo			N/ikas/as-skies
38	VIBR	IA	Vibrator drive
60	C1+	A	Charge pump cap. Positive terminal
58	C1 -	Α	Charge pump cap. Negative terminal
			DC/DC output back-up capacitor positive
61	C2+	Α	terminal

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

36/41

MediaTek Inc.

22	AUDP	IA	Audio positive input			
23	AUDN	IA	Audio negative input			
20	SPK+	OA	Speaker positive output			
21	SPK-	OA	Speaker negative output			
48	BIAS	OA	Bias Bypass			
LED Driv	rer	-				
64	VO_R	IA	R LED current drive			
1	VO_G	IA	G LED current drive			
2	VO_B	IA	B LED current drive			
63	LED_KP	OA	KP LED drive			
62	CS_KP	IA	KP LED current sense			
52	BLDRV	OA	Control output to gate of external FET for back light DC-DC converter			
55	CS_BL	IA	Voltage sense input for external BL FET current			
54	FB_BL	IA	Voltage sense input from white LED ballast resistor			
SPI Inter	face					
40	SPICS	I	Serial port select input			
41	SPICK	I	Serial port clock input			
42	SPIDAT	Ю	Serial port I/O			

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

MediaTek Inc.

5.2 Package





MediaTek Inc.

	Dime	insten in	mm	Dimension in inch		
Symbol	MIN	NOM	MAX	MN	NON	MAX
٨	0.60	0.85	1.00	0.031	0.633	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	1.00	0.024	0.026	0.039
A3		0.20 Ref			0.009 RE	F
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		9.00 ESC			0.354 BS	C
01/E1		8.75 BSI	;	0.344 BSC		
02/E2	5.54	5.69	5.84	0.218	0.224	0.230
8		0.50 BSC	;	0.020 ESC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	۵		1 Z	σ		12
R	0.09	ļ		0.004		
K	0.20	ļ		0.008		
000			0.15			0.006
bbb			0.10			0.004
CCC	—		0.10	—		0.004
ddd	——		0.05			0.002

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

39/41

Commercial Confidential

MediaTek Inc.

5.3 Application Example

A typical application example is shown in following figure 14. Main features are listed as below:

- 1. Charging use USB or AC-DC adaptor.
- 2. Can show charging status during pre-charging in case charging with adaptor power.
- 3. Support power for Memory card.
- 4. Support up to 6 white LEDs for main LCD backlight.
- 5. Support up to 8 LEDs (any color) for keypad illumination.
- 6. Support 3 independent LED drivers (any color).
- 7. Support dim control for all LED drivers.
- 8. Support power for photo sensing circuit.
- 9. Battery removal protection.



Figure 14 Application example

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc. 40/41

MediaTek Inc.

Appendix :

BAT_ON functional circuit example (With BAT temp. sensor) :



Figure 15 BAT_ON connection with Battery Temp. sensor example

Confidential Information

Revision 0.1 – Aug. 3,2004 © 2004 MediaTek Inc.

41/41